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Negative Read Biasing Effects for the Reliable Operation of NOR Type Floating Gate Flash Memory Devices
Seongjae Cho, Il Han Park, Jong Duk Lee, and Byung-Gook Park, Seoul National University

WP9-01-07
Fin Width Variation Effects of Program Disturbance Characteristics on NAND Type Bulk Fin SONOS Flash Memory
Il Hwan Cho, Il Han Park, Hyungcheol Shin, Byung-Gook Park, and Jong Duk Lee, Seoul National University
and Jong-Ho Lee, Kyungpook National University

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* = Nominated for the Best Student Paper Award
Fin Width Variation Effects on Program Disturbance Characteristics in a NAND Type Bulk Fin SONOS Flash Memory

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For the mass storage flash memory, highly scalable device structure should be adopted. As a promising candidate, bulk FinFET SONOS flash memory device has been introduced and reported [1]. Fig. 1 shows the schematic 3-dimentional view of the bulk fin SONOS flash memory device. Fin width is an extra device parameter which is not included in planar device. Effects of fin width on program and erase speed were presented by in previous works [1]. In this study, we report program disturbance characteristics with fin width variation in a NAND type bulk fin SONOS flash memory.

Fig. 2 shows the schematic drawing and bias conditions of NAND array. In a NAND array, the self-boosting scheme is used to prevent program disturbances [2]. The program disturbance of the program inhibited cell which shares the word line with the program cell is determined by the boosted channel potential of the cell. Fin width can change the channel potential because the coupling ratio is related with the fin width. The relationship between program inhibition efficiency and fin width is investigated by device simulation.

To analyze fin width variation effects on program disturbance characteristics, three-dimensional simulation was performed by ATLAS. The simulated NAND array structure is shown in Fig. 3. Two flash cells are connected in series with two select transistors. The fin widths of array are varied from 30 nm to 150 nm and the channel length of memory cell is 100 nm. The oxide-nitride-oxide thicknesses of flash cells are 30 Å /70 Å /50 Å and a the gate oxide thickness of select transistors is 30 Å. The doping concentration of the channel is $2 \times 10^{18} \text{ /cm}^3$ and that of S/D regions is $5 \times 10^{18} \text{ /cm}^3$.

Fig. 4 (a) shows the potential distribution of the cross section (X-Y) of the simulation structure. The potential distribution is varies with position in the channel. The potential around the top of the fin body is higher than that of the other region because the dielectric capacitance is higher due to the triple-gate nature. Channel potential and electric field are influenced by the fin width variation. Fig. 4 (b) shows the potential extracted at the side-channel surface around the side center of fin body as the fin width changes.

This result comes from the ratio of capacitances between the channel and the dielectric. Comparing the channel potential of the devices having fin width of 150nm and 30nm, the latter one has about twice higher channel potential. Dielectric capacitance increases as fin width decreases. Due to the relationship of channel potential and ratio of capacitances, larger boosting efficiency can be achieved by decreasing the fin width so that the program disturbance characteristics will be reduced as shown in Fig. 5.

We have analyzed program inhibition in bulk fin SONOS flash memory devices with a variation of fin body width. Compared to the coupled channel potential of wide fin channel device during programming, the potential of narrow fin structure device was much large. Relationship between the fin width and the program disturbance characteristics can be useful in memory design and optimization.

Acknowledgements
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References


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**Fig. 1:** Schematic diagram of bulk fin SONOS flash memory.

**Fig. 2:** Schematic drawing of a portion of a NAND array and bias condition for program.

**Fig. 3:** Three dimensional simulation structure of NAND type bulk fin flash memory array and cross sections.

**Fig. 4:**
(a) Potential distribution of simulation structure $(L_{gate} = 50 \text{ nm})$
(b) Boosted channel potential with fin width variation

**Fig. 5:** Comparison of self boosting efficiency between a narrow fin device and a wide fin device by a capacitance model of SONOS flash memory.