The Effects of Corner Transistors in STI-isolated SOI MOSFETs

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Abstract

In this work, the effects of corner transistors in SOI MOSFETs were investigated. We fabricated SOI MOSFETs with various widths and a fixed length and characterized them. The SOI thickness was 4000 Å and the buried oxide (BOX) thickness was 4000 Å. The isolation of active region was simply done by silicon etching and TEOS sidewall formation. Several undesirable characteristics have been reported for LOCOS isolation in fabrication on SOI wafers so far. Although we used an STI-like process instead of LOCOS, there were still a couple of abnormal phenomena such as kinks and double humps in drain current. Above all, we investigated the location of the parasitic transistors and found that they were at the corners of the SOI in width direction by high-resolution SEM inspection. It turned out that their characteristics are strongly dependent on the channel width. We made a contact pad through which we can control the body potential and figured out the dependency of operation on the body potential. The double humps became more prominent as the body bias went more negative until the full depletion of the channel where the threshold voltage shift did not occur any more. Through these works, we could get insights on the process that can reduce the effects of corner transistors in SOI MOSFETs, and several possible solutions are suggested at the end.

Index Terms – corner transistor, STI isolation, SOI MOSFETs, drain current kink, drain current hump.

I. Introduction

Recently, SOI-based MOSFETs are used to implement various kinds of discrete devices and related driving circuits. Silicon-on-insulator (SOI) devices are known to have inherent advantages such as better controllability on channel electrons, very low junction capacitance, and soft-error immunity in logic function [1]. In spite of these good qualities, there are difficulties in fabricating SOI devices. These difficulties arise in the isolation process which may result in parasitic transistors in addition to the SOI MOSFETs. When LOCOS isolation method is adopted, there would be a parasitic transistor at the bottom edge of the silicon channel, which lowers the threshold voltage and reduces width due to bird’s beak phenomena originated from LOCOS [2]. To avoid this drawback, shallow trench isolation (STI) is used for betterment, but there can still remain the effects of parasitic transistors residing in the SOI MOSFETs. The representative undesirable characteristics are kinks and double humps in drain current. These phenomena are not genuine features of STI-isolated SOI MOSFETs but characteristics seen in SOI devices that have parasitic components in it. Drain current kinks or double humps should be avoided in that it can cause current overshoots in the devices [3], and they make it very hard to model and to implement circuits. The abnormal characteristics of drain current show width dependency and the effective width of each device is calculated to be longer than the mask active width. The latter is opposite to the results of LOCOS-isolated devices.

In this work, we have fabricated enhancement mode n-type SOI MOSFETs with various widths and a fixed length and characterized them. In addition, we suggest several possible solutions to suppress the effects of corner transistors in SOI MOSFETs.

II. Device Structure

We have fabricated enhancement mode n-type SOI MOSFETs on the buried oxide (SIMOX) of 4000 Å thickness. The widths of the devices are 10, 18, 30, 50, 90, and 120 μm while the length is fixed at 5 μm. Figure 1 shows the top view of the NMOS devices of 90 μm width.

Fig. 1. Fabricated SOI NMOS with W/L = 90 μm/5 μm.

As shown in the figure above, there is a body pad through which we can control the body biasing. Another reason of making the body contact is to reduce the floating body effects of the SOI channel by effectively draining out the accumulated holes due to impact-ionization. The dependency of the drain current characteristics on the negative body bias is to be shown in the next section.
III. Results and Discussion

1. KINKS AND DOUBLE HUMPS IN DRAIN CURRENT

The following figures are $I_d(V_d)$ and $I_d(V_g)$ current characteristics of an NMOS device with $W/L = 90 \mu m/5 \mu m$.

![Fig. 2. Drain current characteristics according to (a) drain voltage and (b) gate voltage (NMOS with $W/L = 90 \mu m/5 \mu m$).](image)

The noticeable features are the kinks in $I_d(V_d)$ characteristics in high drain voltage regions, and double humps in $I_d(V_g)$ characteristics under negative body biases. Both kinks and double humps in drain current can be said as different behaviors of two different MOSFETs, i.e., MOSFETs with different widths and threshold voltages as roughly drawn in Figure 3.

![Fig. 3. Schematic view of parallel connection between two MOSFETs with different widths.](image)

The anomaly in drain current characteristics shown in Figure 2 can be explained by the corner transistor effects. Kinks in $I_d(V_d)$ transfer characteristics are mainly due to the early turn-on and early breakdown of the corner transistors. The elevation of body potential due to the holes in partially depleted SOI channel can also account for the drain current kinks [4]-[5]. Double humps in $I_d(V_g)$ transfer characteristics result from the respective operations of two transistors with different threshold voltages. The $I_d(V_g)$ transfer curve stops shifting about -2.5 V at which the full depletion of channel begin to occur. Until that point, the deformation in characteristic curves gets severer. The low gate voltage region reflects the behavior of the corner transistor which is relatively insensitive to the negative body potential.

2. FINDING DIMENSIONAL FACTOR

Under the assumption that there should be parasitic transistor acting like the one in Figure 2, we did our utmost to find out the location of the parasitic transistor in the MOSFET device. The active region was cut in both length and width direction and investigated by high-resolution SEM. The edge parts of the devices were examined with more caution in the assumption that deposition or etch processes at the cliff of the SOI MOSFET could cause abnormal dimensional profiles.

![Fig. 4. SEM picture of the active region in width direction.](image)

Figure 4 shows the SEM photograph of active region cut in the width direction. There is a parasitic transistor at the top corner of the silicon channel. The SOI is 4000 Å thick and the thermal gate oxide is 250 Å thick. The corner transistor seems to have 1200 Å width along down the cliff of the SOI. This region is formed due to the overetch of TEOS sidewall. After deposition of TEOS sidewall for active isolation, we need to etch back the TEOS before thermal gate oxidation. To make sure to remove TEOS residue on the SOI, it is inevitable to etch TEOS more than initially deposited. Consequently, parasitic transistors are unintentionally constructed on the sidewall spacer.

The width of the corner transistor turns out to be close to 1500 Å. However, the effective width can be more than that, since there might be unknown location of the parasitic components although the undesirable structure is thought to be only along the one side of the active region under our initial design. For this question, we have extracted the effective width of the devices by least-square fit subroutine method. The basic formulation for least-square fitting is as follows. We feed 0.1 V into drain to operate the devices in the linear region and the body contact was grounded.

$$I_d = \frac{W + \Delta W}{L_{ef}} \frac{\mu_s C_m \sqrt{V_{gso}^2 - V_T^2} V_{gs}}{1 + \frac{V_{gs}}{V_T}} A(W + \Delta W),$$

where $A$ is a process constant.
Linear extrapolation method is used for the extraction of threshold voltages to avoid ambiguity that could be brought about due to constant current method. The threshold voltage is 0.77 V, regardless of the channel width. Therefore, when gate voltages were increased from 1 V to 5 V by 1 V, which in turn made the gate over-drive 0.23 V to 4.23 V spaced by 1 V as shown in Figure 5.

3. EVALUATION OF THE MAGNITUDE OF DOUBLE HUMPS

We defined a function that can evaluate the magnitude of double humps in $I_d(V_g)$ characteristics. In the low gate voltage region, current induced by the corner transistor is dominant whereas current is driven by main transistor in high gate voltage region. We can define transition region between these two regions under the effects of different transistors.

![Image](image_url)

Fig. 5. Extraction of effective width through the process dimensional factor.

The drain bias is fixed at 0.1 V. Based on these parameters, since the coefficient $A$ can be regarded as a process constant, it is possible to put $I_d$-$W$ characteristics into first-order lines whose common intercept of the x-axis, i.e., width-axis is the process dimensional factor, $\Delta W$. In case of LOCOS isolation, $\Delta W$ takes a negative value due to the bird’s beak penetration at the bottom edge of the SOI channel, which results in the reduction of effective width of the channel. The common width-intercept is -0.86, which proves that $\Delta W$ is $+0.86 \, \mu m$. This means that the parasitic transistors act like a transistor whose oxide thickness is 250 Å and channel width is 0.86 μm. In short, the corner transistor elongates the main transistor width by this amount.

![Image](image_url)

Fig. 6. $I_d(V_g)$ transfer characteristics according to device channel width.

Figure 6 definitely shows different behavior of discrete NMOS devices. The corner transistor is independent of device channel width, while the main transistor is strongly dependent on it. Since the saturation current increases with the channel width, the wider the channel is, the more prominent does the double hump look.

![Image](image_url)

Fig. 7. Transition region of MOSFETs with double humps

The three points A, B, and C are the points of inflection, which means the second derivative of the characteristic curve becomes zero. Point A is where the drain current gets larger flux due to the turn-on of corner transistor, and C is the point where the current driven by main transistor begins to saturate. Between those two points, there is the point B where the corner transistor current begins to saturate and the main transistor current starts to dominate. From this interpretation, it is reasonable to define the transition region as the voltage interval between points B and C.

![Image](image_url)

Fig. 8. The first and second derivatives of $I_d(V_g)$ characteristics.

The points A, B, and C in Figure 7 are mapped onto the second derivative curve of the drain current characteristic in Figure 8. The dotted line indicates the first derivative and solid line indicates the second derivative. $V_g1$ and $V_g2$ are the gate voltages where the second derivative becomes zero defining the transition region. We defined the magnitude of double humps as the product between the transition region and the corresponding drain current at both ends of the transition region. Longer transition region means larger double hump features and thus the larger drain current difference. Based on these criteria, a function describing the double humps can be
defined as the following formulation:

\[
M = (V_{G2} - V_{G1}) \cdot [I_{DS}(V_{G2}) - I_{DS}(V_{G1})],
\]

(2)

where \( V_{G1} \) and \( V_{G2} \) are the two highest gate voltages at which the inflection of the characteristic curve occur.

Making use of this formulation, the magnitude of humps can be evaluated. Figure 2(b) and Figure 6 infer that double humps in \( I_d(V_g) \) characteristics are varied with both negative body potential and device width. The following two figures prove this hypothesis quantitatively.

**Fig. 9. Hump magnitude according to body-to-source voltages.**

The left vertical axis indicates the transition region length, i.e., \( \Delta V_g = V_{G2} - V_{G1} \), and the right one shows hump magnitudes. According to the definition, the magnitude is in unit of watt. A single n-type MOSFET of 120 \( \mu \)m width was used for characterization represented in Figure 9. Thus, the enlargement of transition region length contributed to the hump magnitude increase than the drain current difference did.

**Fig. 10. Hump magnitudes in devices with different dimensions**

Figure 10 shows dependency of hump magnitude on the device channel widths. It shows monotonic increase as the dependency on negative body potential. However, the contribution of the transition region length is relatively small compared with the previous case in Figure 9 due to the fixed body potential of -1 V. Actually, transition region length has invariance with average of 0.28 V and standard deviation of 0.01 V in calculation.

4. SUGGESTION OF PROCESSES FOR IMPROVEMENT

There can be several ways of reducing the effects of corner transistors. The crucial point is to minimize the step caused by overetch as shown in the dotted circle in Fig. 4. One possible method is deposition of HSQ and successive etch-back. HSQ has smaller viscosity than AZ1512, a representative photoresist, which means that it can readily flow downward the lower regions on the patterned surface. Since HSQ has comparable etch rate to \( \text{SiO}_2 \), if only the process time is well controlled, HSQ in the following etch process can retard the etching of the TEOS sidewall so as to minimize the step. Another possible solution is to use chemical mechanical polishing (CMP). If CMP is conducted on the overall wafer, it grinds the TEOS down to active region with same vertical etch rate, which makes it possible to reduce the step.

IV. Conclusion

In this work, we fabricated SOI MOSFETs and investigated effects of corner transistors. Those parasitic transistors are formed by TEOS isolation and etch-back at the early stage. They result in kinks and double humps in drain current characteristics which can cause erroneous operations. The severity is more prominent for devices with longer width and under more negative body potential. It is recommended that the dimensions are reduced enough so that the anomalies in current characteristics are suppressed under permissible limit. There also can be solutions through adopting other processes. Etch-back after HSQ filling and CMP are the candidates that can minimize the formation of corner transistors.

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References