Double-Recessed Double-Gate MOSFETs for sub-30nm CMOS Technology

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Abstracts – In this work, the effect of the S/D parasitic resistance on the drain current was shown for double gate device. As a candidate to alleviate the S/D parasitic resistance problem, a new double-gate MOSFET with double-recessed channel structure was proposed, and simulated characteristics with recess depth were shown, and showed excellent device characteristics.

I. Introduction

CMOS devices have scaled down to sub-30nm gate-length to achieve high performance and high integration density. Key challenge with the device scaling are non-scalable threshold voltage, high electric field, parasitic source/drain resistance, and VT variation by random dopant distribution[1]. It was well known that double-gate MOS devices among the recent MOSFET structures have shown the best scaling-down characteristics due to the effective suppression of drain electric field by the double-gate structure, and can be scaled down to 15nm channel length[2]. Source/drain region formed in the ultra thin Si width has a large parasitic resistance[3]. Non self-aligned source/drain to gate structure also increases the source/drain parasitic resistance which degrades current drivability[3].

In this paper, we briefly study the effect of contact resistance in DG MOSFETs. Then we propose a new simple DG structure by using a proximity effect of a lithography process, and show simulation results.

II. Effects of Parasitic S/D Contact Resistance

Fig. 1 shows total current density along the center of the source/drain contact position in DG MOSFET. The Si body thickness is 5nm and LG is 20nm. The contact length is 50nm and S/D doping is 1.5×10^20 cm^-3. The insert stands for part of the simulated structure. Process and device simulations were performed by using Silvaco tools[4]. Square and circle symbols represent the current densities for R_C’s of 1×10^-7 Ωcm^2 and 0 Ωcm^2, respectively. The results were obtained along the dashed line in the insert. The current density for R_C of 0 Ωcm^2 decreases significantly from the start (0.05μm) of the S/D contact region, because the current concentrates on the start region of the S/D contact due to the ideal ohmic contact. However, the current density for R_C of 1×10^-7 Ωcm^2 decreases slowly with respect to that of the ideal contact, since the current spreads out along the dashed line due to limitation by the constant resistance. With a R_C of 1×10^-7 Ωcm^2, some of the gate bias drops across the parasitic constant resistance, so the drain current versus the R_C at V_D=V_GS=0.8 V. All device geometry is the same as that in Fig. 1. The device with a R_C of 1×10^-7 Ωcm^2 shows more than 30% degradation over the ideal device.

III. A New DG MOSFET with Double-Recessed Channel

Fig. 3 (a) shows a key experimental result to form the DR channel structure. The SEM view shows the PMMA photoresist pattern formed by e-beam lithography. The photo resist was soft-baked at 150°C for 150sec and developed in MIBK/IPA(1:3) solution for 90sec. A line width of 100nm was designed and the gap between the lines was designed to 50nm. Designed pattern shapes were rectangle. Resultant gap between lines was 40nm and line width was 150nm. We can clearly observe the recessed structure formed by utilizing proximity effect of electron beam. Fig. 4(b) shows the cross-sectional view of the DR DG MOSFET for device simulation. Physical gate length is 20nm and minimum body thickness in the channel region is 5nm which meets the requirement for 15nm gate length. With the double-recess scheme, we can obtain 15nm Si thickness in the S/D region while keeping 5nm Si body thickness in the channel. 15nm thick S/D can lower the parasitic S/D resistance significantly. To check the device performance of the DR DG MOSFET, device simulation was performed.

Fig. 4 shows mask steps for the DR DG MOSFET. In step (a), the gate and the body channel are formed in a mask step, resulting in simple process for the implementation of nano size body and gate. After gate formation, active body for S/D contact is defined as in step (b). Contacts are formed on the vertical sidewall of the body S/D and gate poly-Si, so comparatively large contact area is achieved for nano patterns. The channel is formed on both sides of the vertical sidewall and has a recessed channel on both sides of the sidewall channel.

Fig. 5 shows the subthreshold swing and the drain induced barrier lowering vs. the recessed depth which is defined as the distance presented by arrow marks in the insert. As the depth increases, both SS and DIBL increase. It should be noted that the body thicknesses for the channel center and for the S/D were fixed at 5nm and 15nm, respectively. Small recess depth means that the gate pattern was well defined by optical proximity correction. As the recess depth decreases, overall channel body becomes thin and less concave, which leads to more strong suppression of the drain field by gate field, resulting in smaller DIBL.

Fig. 6 shows I_D-V_GS characteristics of the DR DG NMOSFET with a recess depth of about 46nm. The device
has 20nm gate length and 1nm gate oxide and shows a $V_T$ of 0.34V and excellent SS of 74mV/dec. The DIBL is about 65mV/dec and excellent to be applicable to sub-20nm gate length. By using band-to-band tunneling model, off current at a $V_{DS}$ of 0.8V is obtained to be about $4\times10^{-9}$ A/µm and reasonable.

Fig. 7 shows $I_D$-$V_{DS}$ characteristics of the DR DG NMOSFET. Excellent I-V characteristics were obtained at even relatively large $V_T$ of 0.34V. Effective gate length is about 16nm which is relatively long for conventional 20nm devices, because the channel was recessed. Simulated drain current is about 1mA/µm at $V_{DS}=V_{GS}=0.8V$.

**IV. Conclusion**

The effect of the S/D parasitic resistance on the drain current was shown for double gate device with a body thickness of 5nm. It was shown that the contact resistance is very important for nano scale DG MOSFET. As a candidate to alleviate the S/D parasitic resistance problem, a new double-gate MOSFET with double-recessed channel structure was proposed, and simple mask steps are introduced to implement the structure. Device characteristics with recess depth were shown, and showed excellent device characteristics.

**References**


Fig. 4. Mask steps for the double-recessed DG MOSFETs

Fig. 5. Subthreshold swing and drain induced barrier lowering versus recessed depth. The insert represents the double-recessed DG structure.

Fig. 6. $I_D$-$V_{GS}$ characteristics of 20nm DR double-gate NMOSFET.

Fig. 7. $I_D$-$V_{DS}$ characteristics of 20nm DR double-gate NMOSFET.