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Improving the Cell Characteristics Using SiN Liner at Active Edge in 4 Gbits NAND Flash Memories

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We introduced the self aligned floating poly (SAP) process using the SiN liner at active edge to improve the cell characteristics of high density NAND flash memory devices. Capacitance and electric field at corner of active edge are related to on cell current and cell V_{th} distributions. In a 70 nm design rule NAND flash cell, we can improve the about 0.2 µA of worst on cell current and cell V_{th} distributions of 0.5 V respectively. Furthermore, we acknowledged that off cell current of SiN liner is lower than that of oxide liner. [DOI: 10.1143/JJAP.47.2676]

KEYWORDS: NAND flash, STI, SiN liner, oxide liner, endurance, reliability

1. Introduction

Recently the cell integration density of NAND flash memory is increasing rapidly due to its simple structure suitable for high resolution lithography. Therefore, the reduction of cell size has been the most important issue. However, with the increase in the number of the cells and the scale-down of the cell size, the NAND cell string has some problems such as small on-cell current and poor cell threshold voltage (V_{th}) distributions.[1,2] Also, it was well known that they are related to corner of active edge.[2–4] In this work, we have improved not only the on cell current but also cell V_{th} distributions by using SiN liner to side wall of field oxide.

2. Fabrication of the Memory Cell

The conventional self aligned floating poly (SAP) process flow to form oxide liner to active edge is shown in Fig. 1(a).[5] After pad oxidation, SiN and hard mask is formed and active/field is patterned by lithography and dry etch. After that oxide liner is deposited through low pressure chemical vapor deposition (LP-CVD) as shown in Fig. 1(a-i). As shown in Fig. 1(a-ii), shallow trench isolation (STI) is formed by high density plasma (HDP) and oxide-chemical mechanical polishing (CMP). SiN and pad oxide are removed by wet etch as shown in Fig. 1(a-iii). After tunnel oxide is grown through radical oxidation and polycrystalline silicon (poly-Si) is deposited, floating gate is formed through poly-Si CMP process. After field oxide between floating gates was removed by wet etch, ONO and control-gate is deposited as shown in Fig. 1(a-iv). The new process flow to form SiN liner to active edge is shown in Fig. 1(b). After trench is formed, oxide and SiN liner (50 Å) liner is deposited through LP-CVD as shown in Fig. 1(b-i). In order to conduct oxide-CMP, SiN on active mask is removed by dry etch. As shown in Fig. 1(b-ii), STI is formed by HDP and oxide-CMP. After SiN and pad oxide are removed by wet etch as shown in Fig. 1(b-iii), tunnel oxide and floating gate is formed. The field oxide between floating gates was removed by wet etch down to a level above the top of SiN liner. After that, oxide/SiN/oxide (ONO) and control gate is deposited as shown in Fig. 1(b-iv). The profile of active edge was observed by a scanning electron microscope (SEM) and a transmission electron microscope (TEM). The key parameters for NAND cell array are addressed in Table I. The endurance characteristics of NAND flash cell were measured in test of elements group (TEG) pattern and characteristics of bake retention was conducted in 64 Mbits cell pattern.

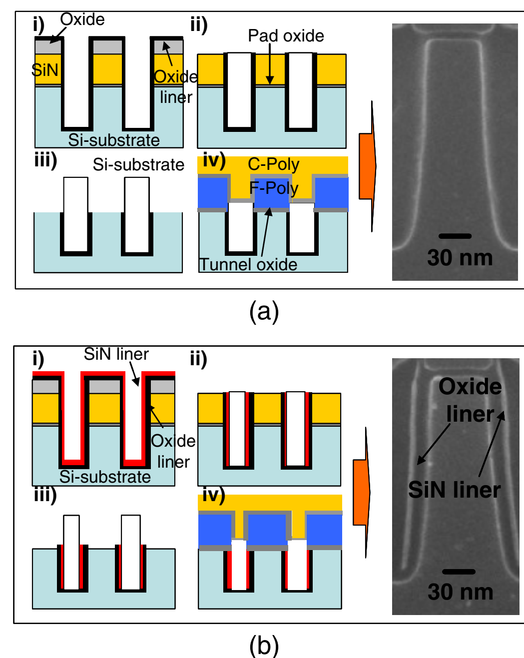

Fig. 1. (Color online) The conventional process flow of (a) oxide liner and (b) SiN liner.

Table I. Key process parameters for 63 nm NAND cell array.

Tunnel oxide (nm)	7
Active width (nm)	65
Gate length (nm)	63
Interpoly ONO thickness (nm)	16.5
Oxide liner thickness (nm)	15
SiN liner thickness (nm)	5

3. Results and Discussion

Figures 2(a) and 3(a) describe the schematic diagram for read operation. Figures 2(b) and 3(b) show the best/worst on

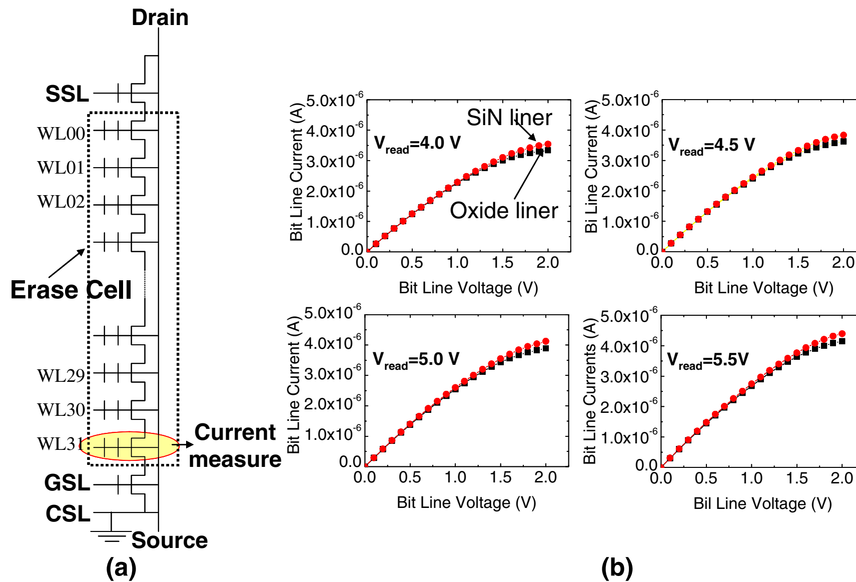

Fig. 2. (Color online) (a) The schematic diagram and (b) the electric characteristics of best on cell current.

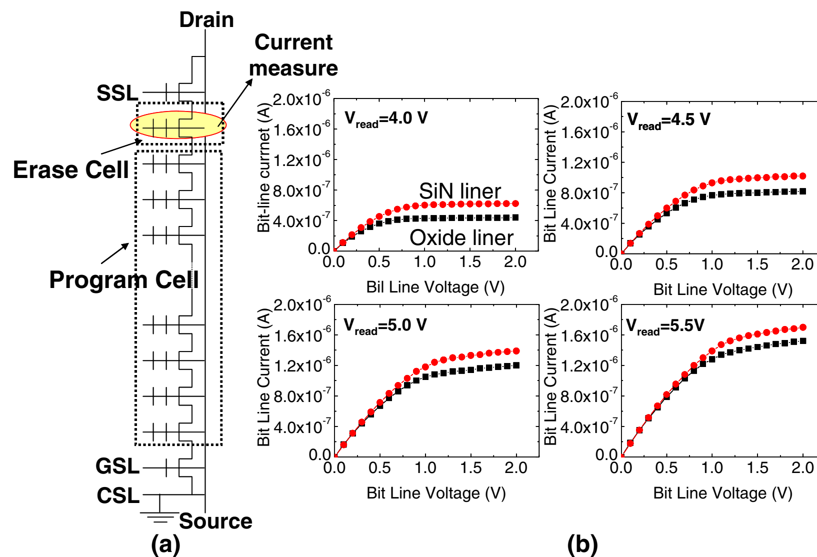

Fig. 3. (Color online) (a) The schematic diagram and (b) the electric characteristics of worst on cell current.

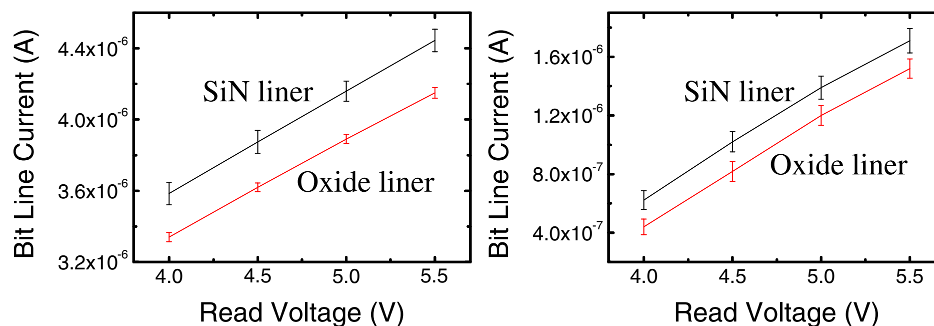

Fig. 4. (Color online) The median and standard deviation value of (a) best on cell current and of (b) worst on cell current at $V_{\text{bit-line}} = 2.0\,\text{V}$.

cell current at read voltage of 4.0, 4.5, 5.0, 5.5 V with oxide and SiN liner. The on cell current of the SiN liner is larger than that of oxide liner due to increased capacitance of tunnel oxide. Figure 4 shows the median and standard deviation value of on cell current respectively at $V_{\text{bit-line}} = 2.0\,\text{V}$. Although the shape and thickness of SiN liner vary near the tunnel oxide, this result explain that the variation do not have an effect on significant difference between SiN liner and oxide liner. Figure 5 shows the simulation results with ATHENA simulator about process in Figs. 1(a) and

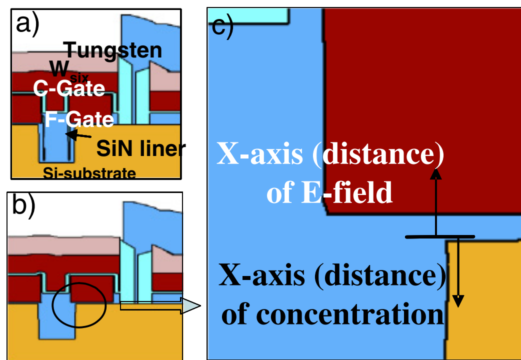

Fig. 5. (Color online) The results of Athena simulation about the process of (a) SiN liner and (b) oxide liner. (c) The measurement point of electric field and concentration.

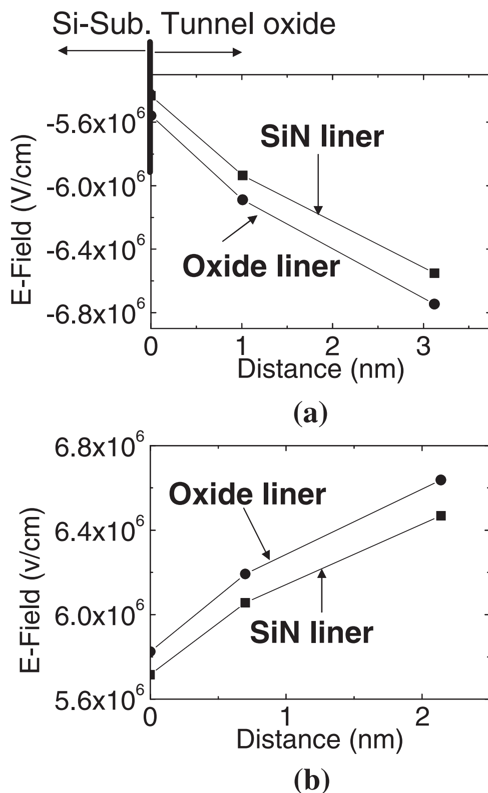

Fig. 6. The electric field of tunnel oxide at active edge for (a) erase state and (b) program state.

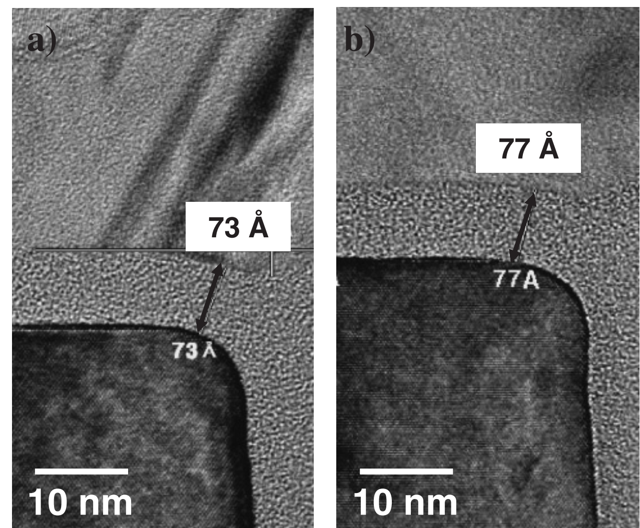

Fig. 7. TEM images of (a) oxide liner and (b) SiN liner at active edge.

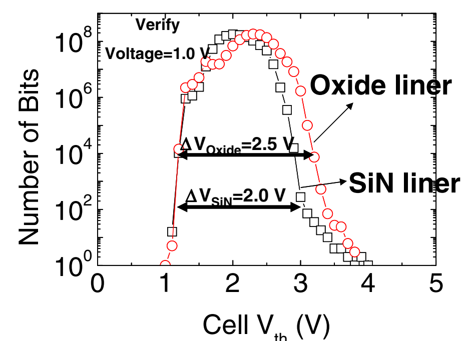

Fig. 8. (Color online) The cell V_{th} distribution characteristics.

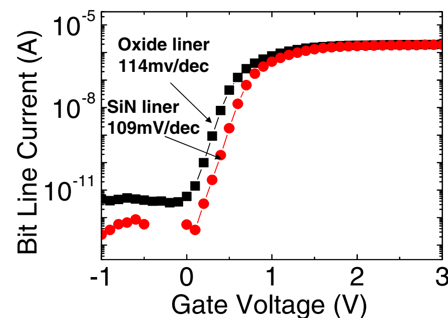

Fig. 9. (Color online) I_d–V_g curves and sub-threshold slope of GSL.

1(b).[6] C_{tun}(SiN liner) = 703 aF and C_{tun}(oxide liner) = 683 aF was obtained from ATLAS simulator for the device in Figs. 5(a) and 5(b), respectively.[6] Also, the electric field at active edge was obtained for erasing and programming state as shown in Figs. 6(a) and 6(b).[6] The electric field at active edge is decreased by SiN liner.[7] Figure 7 shows the active edge profile of tunnel oxide. Oxide thickness of SiN liner process is 4 Å thicker than that of conventional process by SiN liner stress.[8] Figure 8 compares the cell V_{th} distribution of 64 Mbits cell by incremental step pulse program (ISPP). The cell V_{th} distribution was improved with SiN liner due to the decreased electric field and increased thickness of tunnel oxide at active edge.[2] Figure 9 shows the I_d–V_g curves of ground select line (GSL) transistor, which controls the common source line (CSL).[1] The sub-threshold slope of SiN liner is improved due to increased tunnel oxide capacitance. Also, I_{off} of transistor with SiN is decreased. Figure 10 shows the simulation result of boron concentration with oxide and SiN liner. The higher boron concentration around active edge with SiN liner causes the lower I_{off}. The endurance characteristics of SiN liner in comparison to oxide liner are shown in Fig. 11. After 10^5 program/erase cycling at TEG cell, negligible differences in the threshold voltage shift between the SiN liner and oxide liner was observed. Also, as shown in Figs. 12 and 13, bake retention results which are obtained after respectively 5×10^3 and 10^4 program/erase cycles followed by baking at 250 °C for 2 h are improved.

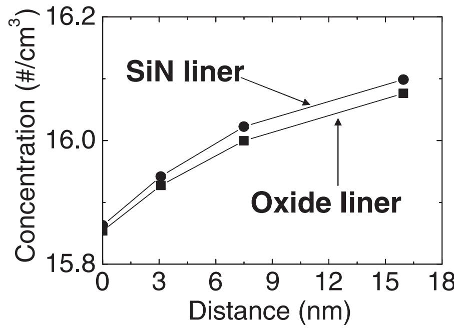

Fig. 10. The boron doping concentration at active edge through the ATLAS simulation.

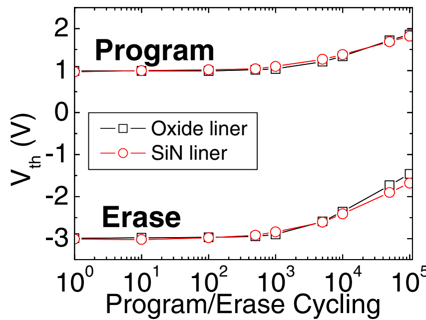

Fig. 11. (Color online) The endurance characteristics after 10^5 program/erase cycling.

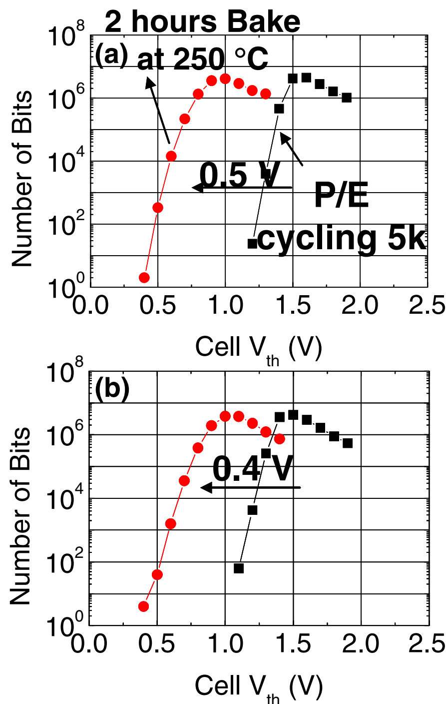

Fig. 12. (Color online) The bake retention characteristics of (a) oxide liner and (b) SiN liner after 5×10^3 program/erase cycling and 250 °C for 2 h.

4. Conclusions

For the first time, we proposed the SAP process using the SiN liner at active edge to improve the cell characteristics of high density NAND flash memory devices. As shown in Table II, the cell current is increased by increased capacitance of tunnel oxide. Also, we could confirm the cell V_{th} distributions are improved due to the decreased electric field and increased tunnel oxide thickness at active edge. The fabricated cell also showed significant improvement in bake retention.

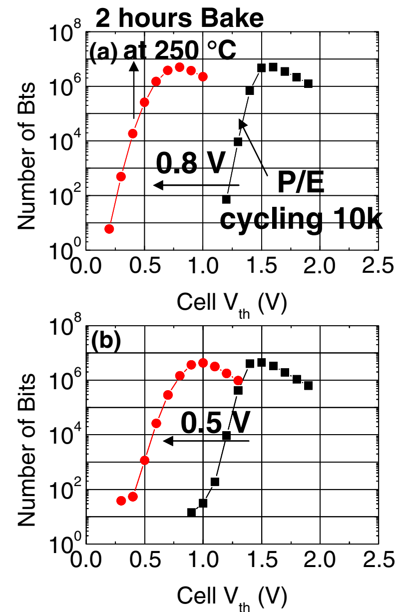

Fig. 13. (Color online) The bake retention characteristics of (a) oxide liner and (b) SiN liner after 10^4 program/erase cycling and 250 °C for 2 h.

Table II. The summary of electrical characteristics.

Type	State	SiN liner	Oxide liner
Cell current (μA)	Worst Situation ($V_{read} = 5.5$ V, $V_{bit\ line} = 1.0$ V)	1.71	1.52
	Best Situation ($V_{read} = 5.5$ V, $V_{bit\ line} = 1.0$ V)	4.41	4.15
I_{off} of GSL transistor (A)	—	5.9×10^{-13}	5.5×10^{-12}
Cell V_{th} distribution (V)	ΔV_{th}	2.0	2.5
Bake retention at 250 °C for 2 h (V)	ΔV_{th} shift (10^4 cycling)	0.5	0.8

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