Admittance Measurements on OFET Channel and Its Modeling With R–C Network

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***Abstract*—For the modeling of charge response behavior in the organic field-effect transistor (OFET) channel, the admittance of the OFET channel is measured from the two-terminal MIS structures. The channel is considered as an R–C network, and both the capacitance and loss of the measured admittance show good agreement with the model. The effective delay of the R–C network depends on the sheet resistance of the channel, the insulator capacitance, and the channel length. The maximum operating frequency of an OFET can be limited by this delay, because the channel charges cannot be induced completely within the delay time.**

***Index Terms*—Admittance measurement, channel, maximum operating frequency, MIS structure, modeling, organic field-effect transistors (OFETs), pentacene, R–C network.**

I. Introduction

FOR THE USAGE of organic field-effect transistors (OFETs) in analog circuits [1], [2], it is important to study the limits of device performance and the origin of the limits. For decades, field-effect mobility has been a good indicator to evaluate the performance limits of OFETs, because it determines the maximum dc current level when the amount of channel charge is given. However, for the ac operation of OFETs, more detailed analyses on those limits are still on demand.

The admittance of organic devices has been investigated to obtain charge density [3], carrier concentration [4], or interface trap properties [5]. It has also been a useful tool to build a small-signal model of devices [5], [6], because both the resistive and reactive characteristics of a device can be obtained from the measurements. Although capacitance measurement on OFET channel has been done to determine the intrinsic mobility of device [7], [8], there has been no trial to measure and analyze the resistive part of the channel admittance. In this letter, both the resistive and reactive parts of the channel admittance are measured, and the values are compared to the R–C network modeling results. In addition, the implication of the modeling results is discussed relating to the maximum operating frequency of OFETs.

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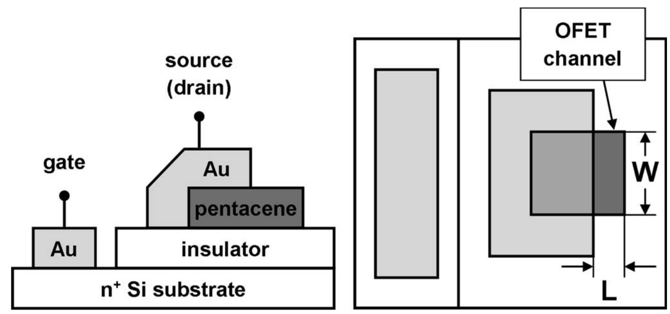

Fig. 1. Cross-sectional view and top view of the fabricated devices. For the admittance measurement on the channel, two-terminal MIS structures with the OFET channel are fabricated. One electrode is gate, and the other electrode is either source or drain.

II. Experiments

For the admittance measurements on OFET channel, two-terminal MIS structures which can be considered as half of OFETs are fabricated, as shown in Fig. 1. Due to its symmetry, the admittance of OFET channel would be twice of the measured admittance. An n^+-Si wafer with a sheet resistance of 10 Ω/sq is used as the gate electrode, and a 35-nm-thick thermal SiO_2 with a dilute polymethyl–methacrylate treatment [9] is used as the insulator. After the pentacene film of 50 nm is thermally evaporated through shadow mask, another electrode which can be considered as either source or drain is e-gun evaporated with gold. The channel length L of 15–95 μm with a 10-μm interval is obtained by intentional misalignment between the pentacene and the gold masks, and the channel width W is 470 μm. Admittance is measured in air with the HP4284A LCR meter with a frequency of 100 Hz–1 MHz and a dc gate voltage of -10 to 10 V. The admittance of the channel is obtained from the total admittance by subtracting the estimated gate–source overlap admittance. To calculate the gate–source overlap admittance with its area, the dedicated devices for admittance calculation are fabricated in the same substrate. More detailed description can be found in [10].

III. Results and Discussion

To model the channel admittance, the R–C network is adopted, as shown in the inset of Fig. 2(a). Under negative dc gate bias, the resistance R is assumed to be uniform along the whole channel, because the amount of the accumulated holes does not change considerably by the ac small signal during the admittance measurements. The capacitance C can be approximated to the insulator capacitance C_i if enough

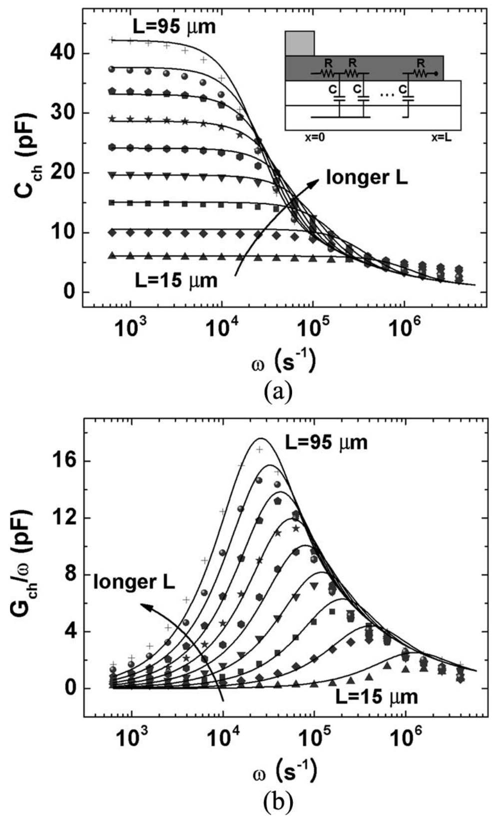

Fig. 2. (a) Channel capacitance C_{ch} (dotted line) measured at $V_G = -10$ V and the calculated C_{ch} (solid line) from the R–C network model show good agreement. The R–C network model of OFET channel is depicted in the inset. (b) Channel loss G_{ch}/ω (dotted line) measured at $V_G = -10$ V and the calculated G_{ch}/ω (solid line) from the R–C network model show good agreement.

holes are accumulated at the interface. The resistance in the n^+-Si gate electrode and contact resistance is assumed to be negligible, because the resistance R in the channel is large enough in this experiment. In analogy with the small-signal gate resistance model of silicon MOSFETs [11], [12], the channel admittance $Y_{\text{ch}}(\omega, L)$ can be expressed as

$$Y_{\text{ch}}(\omega, L) = G_{\text{ch}}(\omega, L) + j\omega C_{\text{ch}}(\omega, L) \tag{1}$$

$$\frac{G_{\text{ch}}(\omega, L)}{\omega} = \frac{C_i L W}{\sqrt{2C_i R_{\text{sh}} L^2 \omega}} \times \frac{-\sin\sqrt{2C_i R_{\text{sh}} L^2 \omega} + \sinh\sqrt{2C_i R_{\text{sh}} L^2 \omega}}{\cos\sqrt{2C_i R_{\text{sh}} L^2 \omega} + \cosh\sqrt{2C_i R_{sh} L^2 \omega}} \tag{2}$$

$$C_{\text{ch}}(\omega, L) = \frac{C_i L W}{\sqrt{2C_i R_{\text{sh}} L^2 \omega}} \times \frac{\sin\sqrt{2C_i R_{\text{sh}} L^2 \omega} + \sinh\sqrt{2C_i R_{\text{sh}} L^2 \omega}}{\cos\sqrt{2C_i R_{\text{sh}} L^2 \omega} + \cosh\sqrt{2C_i R_{\text{sh}} L^2 \omega}} \tag{3}$$

where C_i, R_{sh}, L, and W represent the insulator capacitance per unit area, the sheet resistance of the channel, the channel length, and the channel width, respectively.

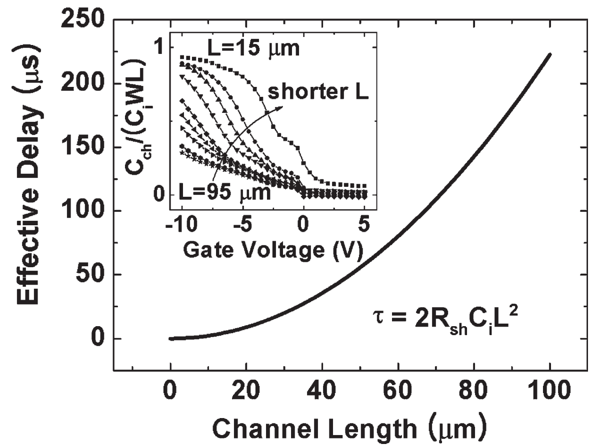

Fig. 3. Effective delay τ which is needed to induce charge in the channel by small gate signal has parabolic relation with the channel length L. To calculate τ, the values of R_{sh} and C_i obtained from the modeling are used. In the inset, C_{ch} measured at 10 kHz as a function of gate voltage is normalized by the maximum channel capacitance $C_i W L$. For high frequency operation, L should be short to fully induce charges in the channel.

In Fig. 2, the measured admittance at the gate bias of -10 V with different channel lengths is compared to the R–C network modeling results. At $V_G = -10$ V, enough holes are accumulated at the interface to make a channel, and their response to the gate small signal makes admittance, i.e., capacitance C_{ch} and loss G_{ch}/ω. At low frequency, measured C_{ch} is proportional to L, because the whole channel can fully respond to the gate small signal. C_{ch} starts to decrease after a certain ω depending on L, while a peak is observed in G_{ch}/ω at the same ω. The R–C network modeling explains this observation clearly, as shown in the figure with solid lines. For the modeling, C_i of 95.8 nF/cm^2 and R_{sh} of 11.63 MΩ · sq are used, and good agreement is observed in both the C_{ch} and G_{ch}/ω curves, which verify the effectiveness of the R–C network model.

The charges in OFET channel cannot be induced instantaneously with the gate-voltage change, so the charge response time can be a bottleneck in high frequency operation of the device. From the above modeling results, the time needed to make the charges induced in the channel can be expressed with the effective RC delay

$$\tau = 1/\omega = 2R_{\text{sh}} C_i L^2 \tag{4}$$

where 97% of the total charges are responding in the channel within τ. In Fig. 3, the delay τ is depicted with the channel length L using the values of R_{sh} and C_i from the modeling. When the operating frequency of one device is given, the curve can be used to determine L. For example, L should be less than 27 μm from the figure for the 10-kHz operation of a device. To verify this estimation, C_{ch} is measured at 10 kHz as a function of gate bias and is normalized by the $C_i W L$ in the inset of Fig. 3. When $L = 15$ μm, the channel capacitance almost recovers $C_i W L$ at $V_G = -10$ V, but longer devices cannot fully induce charges at this frequency. On the contrary, the curve can give the maximum operating frequency when the minimum channel length is given, e.g., 7.14 MHz for $L = 1$ μm in this experiment. There are three ways to reduce this delay.

First, to decrease R_{sh}, the mobility or the carrier concentration should be enhanced. Second, small C_i should be used, but it can cause low on-current or low transconductance. Third, as the most reasonable approach, the channel length of the device should be scaled down.

IV. Conclusion

The admittance of OFET channel is measured and modeled with the R–C network. Both the measured capacitance and the loss curve show good agreement with the theoretical expectations. Therefore, the R–C network model can explain the charge response behavior of the OFET channel. The effective RC delay due to the R–C network can be one of the factors which restricts the maximum operating frequency of OFETs.

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