

Grain size effects on contact resistance of top-contact pentacene TFTs

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Abstract

Multiple top-contact OTFTs with various channel lengths (L_c) were successfully scaled-down to the L_c of 1.8 μm by using the membrane shadow mask and the interface between the evaporated Au and pentacene was analyzed based on the channel resistance method. For large grain pentacene (S-80) deposited at 80 °C, the parasitic resistance (R_p) at $V_{GS} = -20$ V has 1.8 ± 0.2 k Ω cm, whereas for small grain pentacene (S-20) deposited at 20 °C has 4.2 ± 0.2 k Ω cm, which means that R_p depends on the grain size of pentacene. The grain size and grain boundary trap density for pentacene can be possibly origins to determine R_p , which is critically correlated with bulk transport in pentacene. The grain boundary trap density (N_t) for S-80 and S-20 was extracted as $(5.6 \pm 0.5) \times 10^{11}$ and $(1.2 \pm 0.3) \times 10^{12}$ cm $^{-2}$ from the Levinson plots, respectively. In addition, activation energy of R_p for S-80 is in the range from 42 to 48 meV, whereas for S-20 is from 72 to 108 meV.

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1. Introduction

Recent progress in organic thin film transistors (OTFT) technology has led to charge carrier mobility comparable to amorphous silicon [1,2]. Among various organic semiconductors, pentacene has shown the highest OTFT mobility (>1 cm 2 /V s) to date, and has nearly reached the intrinsic transport limit of organic single crystals [3,4]. Despite this considerable progress, few efforts [5–8] have been made to investigate contact effects in organic transistors, compared with scientific trials directed towards larger field effect mobilities.

Consequently, the charge injection/extraction process at the source/drain electrodes is still relatively poorly understood. This is somewhat surprising since contact resistances in organic transistors are typically in the range from 10 k Ω cm to 10 M Ω cm compared to their inorganic counterparts. That is due to the fact that the source and drain contacts in organic TFTs are not easily optimized by conventional processes such as selectively semiconductor doping [7]. Therefore, understanding the electrical properties of the contacts and their dependence on electrode materials, organic semiconductors, and processing

conditions is therefore clearly important from this engineering perspective.

Among two configuration (i.e., bottom- or top-contact) of OTFTs, top-contact devices that use metal electrodes evaporated on top of a semiconductor film are one of the most commonly used designs, but the standard patterning technique (i.e., shadow masking) is hardly capable of high resolution [9]. Thus, the contact resistance calculation based on the empirical model by Luan and Neudeck [10] and Kanicki et al. [11] are rarely used to investigate the interface between the evaporated metal and the semiconductor in the top contact devices, even though their contact resistances are critically important and presumably influenced by the morphology of organic semiconductor and the degree of metal penetration into the semiconductor [12,13].

In this study, scaling-down of top-contact pentacene TFTs was accomplished up to 1.8 μm by using Si nitride membrane shadow mask [14] in order to apply the empirical model to top-contact OTFTs. For OTFTs with different pentacene grain size, comparative analysis for the parasitic resistance (R_p) is performed based on the empirical model to elucidate the grain size effects on contact resistance. In addition, variable temperature measurements [8], which provide information about trap states and their distributions in the semiconductor were executed in order to get insight into the origins to determine R_p .

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2. Experiments

Fig. 1(a) shows a schematic illustration for the fabrication of top-contact pentacene TFTs (OTFTs). OTFTs were fabricated on a p-type wafer with the resistivity of $15 \Omega \text{ cm}$. Thirty-five-nanometre thick oxide was thermally grown on a p-type wafer. The thermal oxide was patterned by photolithography, and then

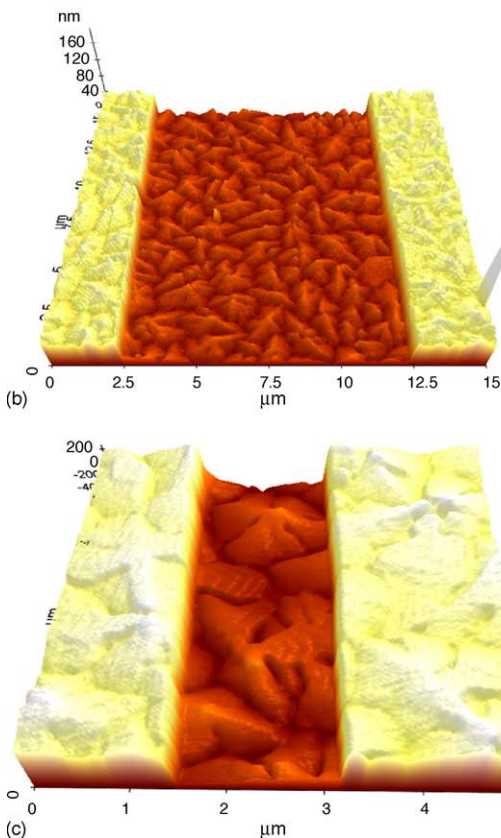
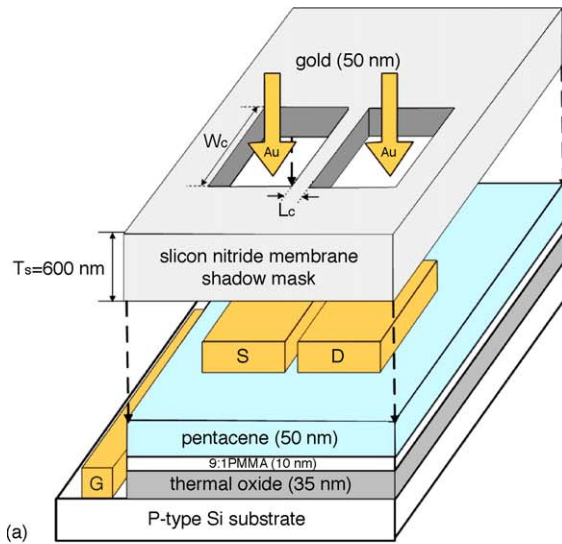


Fig. 1. (a) Schematic illustration of process steps for pentacene TFTs fabricated using a silicon nitride membrane shadow mask. AFM images for channel area of pentacene TFTs with channel length (L_c) of: (b) $10 \mu\text{m}$; and (c) $1.8 \mu\text{m}$. Pentacene was deposited at substrate temperature (T_s) of 80°C .

etched by dilute HF solution for a contact of gate electrode. After surface modification by dilute PMMA solution [15], the as-received pentacene (Sigma–Aldrich) with only 97% purity was sublimated several times from a resistively heated quartz crucible and then deposited on the main samples with the PMMA treated oxide under the vacuum level of 10^{-8} Torr.

In order to investigate into the grain size effects on the contact resistance for OTFTs, deposition condition of pentacene was split into two. One for sample-20 (S-20) is substrate temperature (T_s) of 20°C , pentacene thickness (t_p) of 50 nm, and deposition rate of 0.3 \AA/s . The other for sample-80 (S-80) was thermally deposited at the same conditions of S-20 except T_s of 80°C . Through the Si nitride membrane shadow mask [14], 50 nm-thick-gold was e-gun evaporated on the pentacene layer to define S/D electrodes of OTFTs with the channel width (W_c) of $150 \mu\text{m}$ and the L_c ranging from 20 to $1.8 \mu\text{m}$. As shown in Fig. 1(b and c), the surface morphology of pentacene and physical dimension for the fabricated OTFTs were studied with atomic force microscopy (AFM). The AFM images indicate that for the fabricated OTFTs, the representative channel with 10 and $1.8 \mu\text{m}$ was clearly defined on the pentacene layer among various channel lengths ranging from 20 to $1.8 \mu\text{m}$ despite the usage of shadow mask.

For the fabricated OTFTs, all electrical measurements for OTFTs without passivation were performed in air by using Agilent 4156B electrical parameter analyzer. In addition, transfer characteristics for two samples in the linear regime were measured at various temperatures from 293 to 323 K with the step of 10 K to investigate into the activation energy for contact resistance.

3. Results and discussion

In the linear regime of $V_{DS} = -3 \text{ V}$, the transfer characteristics for an S-20 and an S-80 were shown in Fig. 2. As shown in Fig. 2(a and b), the current level was significantly increased as L_c was reduced from 10 to $1.8 \mu\text{m}$. From the transfer characteristics in the linear regime, the extracted electrical parameters for OTFTs with $L_c = 10 \mu\text{m}$ and $L_c = 1.8 \mu\text{m}$ were summarized in Table 1. For OTFTs with $L_c = 10 \mu\text{m}$, the effective mobility (μ_{lin}), threshold voltage (V_{th}), current on-off (I_{on}/I_{off}) ratio and subthreshold slope (SS) for S-80 were $0.359 \pm 0.002 \text{ cm}^2/\text{V s}$, $-7.849 \pm 0.173 \text{ V}$, $(4.5 \pm 1.7) \times 10^5$, and $2.25 \pm 0.17 \text{ V/dec}$, whereas for S-20 were $0.138 \pm 0.002 \text{ cm}^2/\text{V s}$, $-8.528 \pm 0.029 \text{ V}$, $(3.4 \pm 0.2) \times 10^5$, and $2.37 \pm 0.15 \text{ V/dec}$, respectively. The result denotes that the mobility for S-20 is approximately 3 times larger than that of S-20, which is likely due to the grain size effects [16].

For the scaled-down OTFTs with $L_c = 1.8 \mu\text{m}$, electrical parameters for S-80 were extracted as $0.112 \pm 0.001 \text{ cm}^2/\text{V s}$, $-7.421 \pm 0.239 \text{ V}$, $(2.9 \pm 1.4) \times 10^4$, and $2.63 \pm 0.18 \text{ V/dec}$ and for S-20 as $0.052 \pm 0.001 \text{ cm}^2/\text{V s}$, $-8.152 \pm 0.054 \text{ V}$, $(8.0 \pm 0.5) \times 10^5$, and $2.63 \pm 0.17 \text{ V/dec}$. As the channel length was reduced from 10 to $1.8 \mu\text{m}$, the deteriorated mobility is due to the fact that contact resistance dominated the overall device resistance [6]. In addition, compared with S-20, the reduced

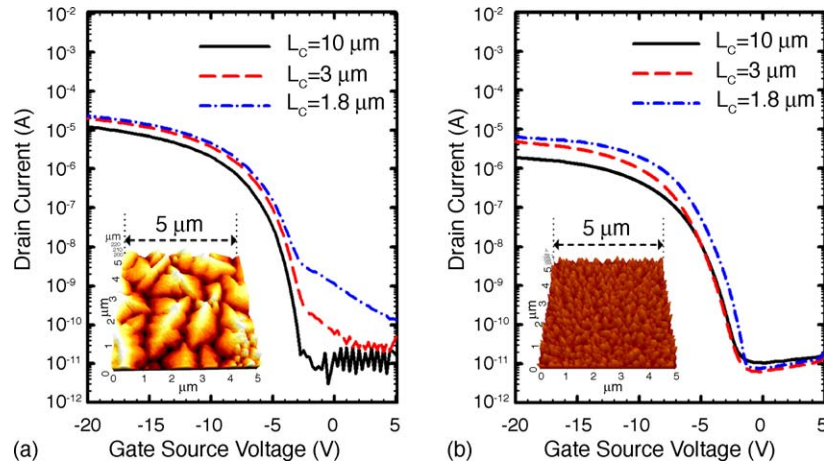


Fig. 2. (a) Transfer characteristics for pentacene TFTs with deposition condition of: (a) $T_s = 80^\circ\text{C}$; and (b) $T_s = 20^\circ\text{C}$ in the linear regime ($W_c = 150\ \mu\text{m}$, $L_c = 10, 3, \text{ and } 1.8\ \mu\text{m}$, $V_{DS} = -3\ \text{V}$). The inset in (a) and in (b) shows the AFM image of pentacene deposited at 80 and 20°C . AFM images indicate that the grain size of pentacene deposited at 80 and 20°C is in the range from 2 to $4\ \mu\text{m}$ and from 0.2 to $0.3\ \mu\text{m}$, respectively.

$I_{\text{on}}/I_{\text{off}}$ ratio for S-80 device can be ascribed to various reasons [17] such as pentacene conductivity, interdiffusion of gold, parasitic resistance, and locally ill-defined S/D edge as the channel length decreases.

As shown in the inset of Fig. 2(a and b), the AFM images for pentacene grain size confirm the result of field effect mobility. On the other hand, the increase of anomalous off-current in the depletion regime was reproducibly observed for the large grain OTFTs as the channel length decreases to the size of pentacene grain, whereas the similar behavior of off-current was not observed for small grain OTFTs even with $L_c = 1.8\ \mu\text{m}$. Among various reasons, the contact resistance for OTFTs can be one of main candidates to govern the off-current in the depletion regime. Therefore, it is meaningful to investigate into the pentacene grain size dependency on the contact resistance of OTFTs.

The dependence of the current/voltage characteristics on channel length can be used to extract parasitic resistances that include various components related to the contacts. In the linear regime, the overall device resistance (R_{on}) can be expressed as the sum of the intrinsic channel resistance (R_{ch}) and a parasitic resistance (R_p) according to

$$R_{\text{on}} = \left. \frac{\partial V_{DS}}{\partial I_{DS}} \right|_{V_{DS} \rightarrow 0}^{V_G} = R_{\text{ch}} + R_p = \frac{L}{W\mu_i C_i (V_G - V_{Ti})} + R_p, \quad (1)$$

where μ_i and V_{Ti} are the intrinsic mobility and threshold voltage, respectively [6]. The parasitic resistance (R_p) can be extracted by determining R_{on} from the linear regime of the transfer charac-

teristics and plotting the width-normalized $R_{\text{on}} \cdot W$ as a function of L for different gate voltages.

In addition, the inset in Fig. 3(a) shows that R_p can be equivalently expressed as the sum of four components such as sR_i , sR_b , dR_b , and dR_e , where sR_i and dR_e originate from the charge carrier injection/extraction process in the S/D electrodes and sR_b and dR_b are due to the bulk transport in the pentacene before the injected charge carriers from S/D electrodes reach the accumulation layer at the insulator/pentacene interface [7]. From the empirical model developed by Luan and Neudeck [10] and Kanicki et al. [11], the $R_p \cdot W$ can be equivalently to the minimum effective contact resistance ($(R_p \cdot W)_0$) in series with an accumulation channel of length l_0 under the source/drain electrodes. Among the previously mentioned four components, the sum of sR_i and dR_e can be linked to the value of $(R_p \cdot W)_0$, which is the minimum effective contact resistance with the characteristics of independence on gate voltage. The linkage $(R_p \cdot W)_0$ to the injection/extraction term of sR_i and dR_e is thought to be reasonable due to the fact that thermionic emission of carriers over the injection barrier does not explicitly depend on applied voltage, even if there can be second-order field-induced barrier lowering effects [18].

Fig. 3 shows that $(R_p \cdot W)_0$ for S-80 and S-20 was extracted as 0.2 and $1.2\ \text{k}\Omega\ \text{cm}$, respectively. The result for $(R_p \cdot W)_0$ may be attributed to the difference in the effective channel width (W_{eff}). The surface roughness for S-20 is larger than that of S-80 due to the nanoscopic morphology difference between S-20 and S-80. The rougher surface with smaller grains leads to an enlarged contact area between gold and the pentacene layer,

Table 1
Electrical parameters for OTFTs deposited at substrate temperatures (T_s) of 20 and 80°C

T_s ($^\circ\text{C}$)	L_c (μm)	V_{th} (V)	μ_{lin} ($\text{cm}^2/\text{V s}$)	$I_{\text{on}}/I_{\text{off}}$ ratio	Subthreshold slope (V/dec)
20	10	-8.528 ± 0.029	0.138 ± 0.002	$(3.4 \pm 0.2) \times 10^5$	2.37 ± 0.15
80	10	-7.849 ± 0.173	0.359 ± 0.002	$(4.5 \pm 1.7) \times 10^5$	2.25 ± 0.17
20	1.8	-8.152 ± 0.054	0.052 ± 0.001	$(8.0 \pm 0.5) \times 10^5$	2.63 ± 0.17
80	1.8	-7.421 ± 0.239	0.112 ± 0.001	$(2.9 \pm 1.4) \times 10^4$	2.63 ± 0.18

L_c and T_s indicate channel length and substrate temperature, respectively.

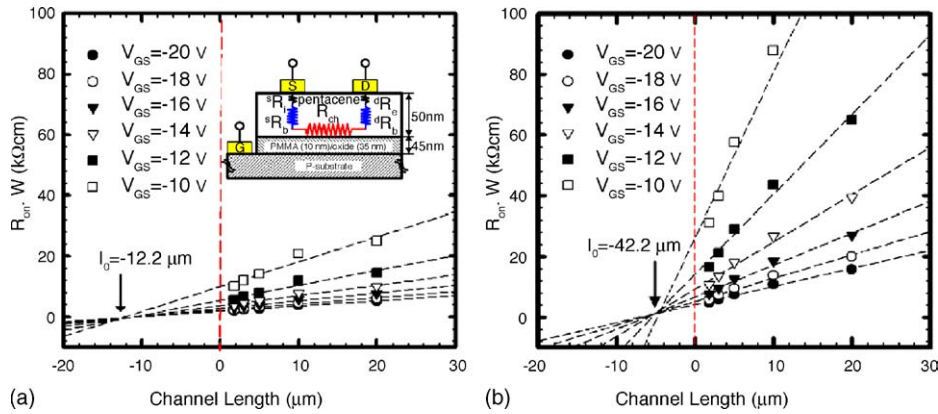


Fig. 3. Width normalized device resistance ($R_{on} \cdot W$) as a function of channel length (L_c) at $V_{DS} = -3$ V and V_{GS} from -10 V to -20 V. $R_{on} \cdot W$ was extracted from OTFTs deposited at: (a) 80°C ; and (b) 20°C with channel lengths between 1.8 and $20\ \mu\text{m}$ and W_c of $150\ \mu\text{m}$. The y-intercepts of the fitted dashed lines give the parasitic resistances at the various gate voltages. All fitted lines meet at a single point, which defines a characteristic normalized resistance $(R_{on} \cdot W)_0$. $(R_{on} \cdot W)_0$ has $0.2\ \text{k}\Omega\ \text{cm}$ at $l_0 = 12.2\ \mu\text{m}$ in (a); and $1.2\ \text{k}\Omega\ \text{cm}$ at $l_0 = 4.2\ \mu\text{m}$ in (b). The inset in (a) indicates a simplified low-frequency equivalent pentacene TFT circuit where the conducting path between source and drain is divided into a series of five resistive elements of sR_i , sR_b , R_{ch} , dR_b , and dR_e .

which means that the W_{eff} for S-20 is naturally longer than that of S-80. Therefore, the large W_{eff} for S-20 can result in the larger $(R_p \cdot W)_0$ than that of S-80.

Fig. 3 shows that the parasitic resistance corresponds to the y-axis intercept of the extrapolated linear fit of $R_{on} \cdot W$ versus L . This resistance depends on the gate voltage as shown in Fig. 4(a). The same gate voltage dependency on parasitic resistance is also reported in recent publication [19]. Fig. 4(a) shows that the parasitic resistance of S-80 is about 3 times larger than that of S-20. For the device of S-80, a width-normalized contact resistance is $1.8 \pm 0.2\ \text{k}\Omega\ \text{cm}$ at the gate voltage of -20 V and $10.0 \pm 0.5\ \text{k}\Omega\ \text{cm}$ at -10 V. For the device of S-20, a width-normalized contact resistance is $4.2 \pm 0.2\ \text{k}\Omega\ \text{cm}$ at the gate voltage of -20 V and $26 \pm 0.7\ \text{k}\Omega\ \text{cm}$ at -10 V. The result indicates that the parasitic resistance is closely related with grain size of pentacene though Au deposition for two samples was performed in the same batch. In a sense, there is a recent report for the grain size dependency on R_p studied by Pesavento et al. [20], utilizing gated four-probe measurements, which are known to have a similar result [8] compared with the parasitic resistance determined from R versus L plots. For the reported OTFTs with

large pentacene grain on SiO_2 gate insulator, the R_p at high V_{GS} by using four probe measurements is estimated as $2.25\ \text{k}\Omega\ \text{cm}$ in the literature, which is a similar value of $1.8 \pm 0.2\ \text{k}\Omega\ \text{cm}$ for S-80 in this study. The results hint that the magnitude of the extracted R_p and the observed grain size dependency on R_p in this study might be reasonable.

Thus, it is meaningful to investigate into the origins of the grain size effects on the R_p of pentacene TFTs. In order to elucidate the above mentioned origins, it is highly required to analyze the relationship between four components of R_p and grain size of pentacene.

Among four components of R_p , R_p is mainly caused by sR_b and dR_b because sR_i and dR_e are much smaller than R_p . In addition, the dependency of R_p on V_{GS} is mainly originated from components such as sR_b and dR_b , which is substantiated by the fact that thermionic emission, which is dominant process for injection of charge carriers in OTFTs, does not explicitly depend on field as mentioned previously [18].

Obviously, since R_p is mainly caused by the components, i.e., sR_b and dR_b , related with the bulk transport in the pentacene, R_p is critically determined by the bulk mobility [7], which is closely

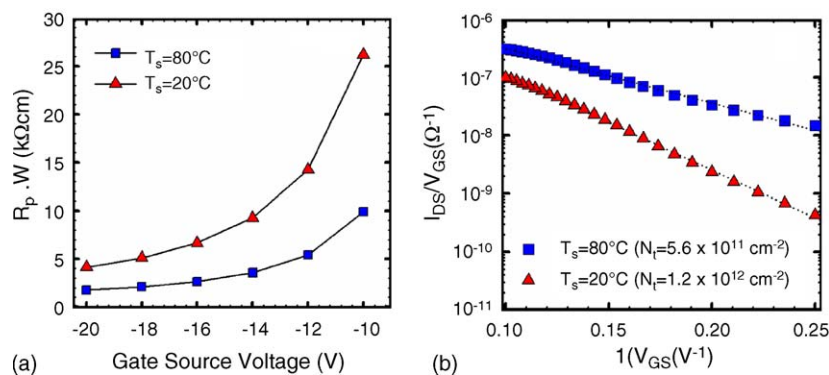


Fig. 4. (a) Width normalized parasitic resistance ($R_p \cdot W$) as a function of gate voltage for OTFTs with pentacene deposited at 80 and 20°C . The values of $R_p \cdot W$ were extracted from analysis of devices with channel lengths between 1.8 and $20\ \mu\text{m}$ and a fixed channel width of $150\ \mu\text{m}$. (b) Levinson plot $[\ln(I_{DS}/V_{GS})$ vs. $1/V_{GS}]$ for OTFTs with pentacene deposited at 80 and 20°C . For two samples, the trap density at the grain boundary can be estimated to be $(5.6 \pm 0.5) \times 10^{11}$ and $(1.2 \pm 0.3) \times 10^{12}$ from the slopes, respectively.

related with the grain size and the trap states localized mainly at grain boundaries. In order to examine the relation between R_p and grain boundary trap density (N_t), N_t is extracted by using the Levinson technique [21]. From the approximated the drain current I_{DS} equation,

$$\ln\left(\frac{I_{DS}}{V_{GS}}\right) = \ln\left(\frac{W\mu_{GBO}V_D C_i}{L}\right) - \frac{eN_t^2 t}{8\epsilon_r\epsilon_0 kTC_i} \left(\frac{1}{V_{GS}}\right), \quad (2)$$

where W , L , and t are the channel width, length, and the thickness of polycrystalline film, respectively. From the slopes in Fig. 4(b), N_t for the devices of S-80 and S-20 was estimated to be $(5.6 \pm 0.5) \times 10^{11}$ and $(1.2 \pm 0.3) \times 10^{12} \text{ cm}^{-2}$, respectively. The grain boundary trap density (N_t) for S-20 is about two times as large as that of S-80. As shown in the inset in Fig. 2(a and b), the pentacene grain size for S-80 is in the range from 2 to 4 μm , whereas for S-20 in the range from 0.2 to 0.3 μm . The result clearly substantiates the fact that the grain boundary trap density (N_t) decreases as the grain size of pentacene increases. Therefore, the parasitic resistance of R_p decreases as the grain size increase. The results indicate that the difference of R_p for S-80 and S-20 can be caused by the possible origins such as grain size and grain boundary trap density.

On the other hand, Fig. 4(a) shows that $R_p \cdot W$ has the dependency of gate-source voltage. The result needs to be investigated in order to get insight into the grain size effects on the parasitic resistance of OTFTs. In the linear regime of OTFTs ($V_{DS} = -3 \text{ V}$), variable temperature TFT measurements ranging from 293 to 323 K were executed to obtain an Arrhenius plot of parasitic resistance of OTFTs with different grain size. The investigation of activation energy for R_p is based on the assumption, which means that a consequence of assuming multiple trapping and release (MTR) model with an exponential distribution of trap states is that the Meyer-Neldel Rule (MNR) should hold. The MNR relates

$$G = G_0 \exp\left(\frac{-E_A}{kT}\right) \quad (3)$$

$$G_0 = G_{00} \exp\left(\frac{E_A}{kT_0}\right) \quad (4)$$

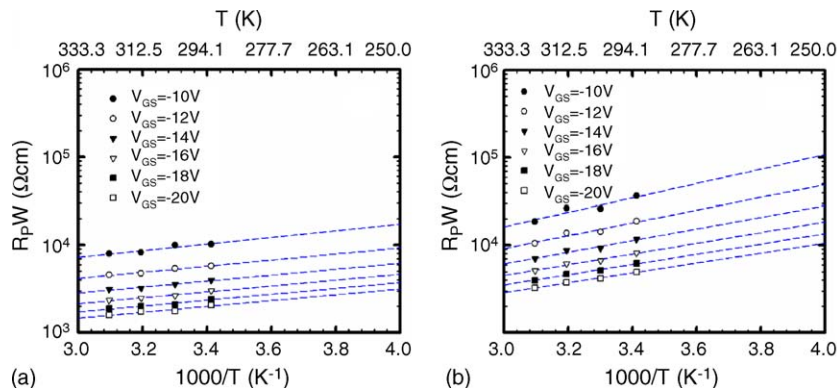


Fig. 5. Arrhenius plots of width normalized parasitic resistance obtained from OTFTs with pentacene deposited at: (a) 80 °C; and (b) 20 °C. The dashed lines are the results of the least squares fittings to Arrhenius relation for the respective gate voltage.

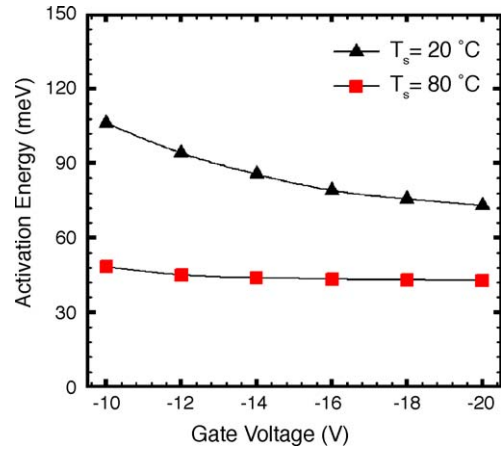


Fig. 6. Activation energy for width normalized parasitic resistance as a function of gate voltage. The solid triangles and squares correspond to the cases of OTFTs with pentacene deposited at 80 and 20 °C.

between an electrical property G , its activation prefactor (G_0) and the activation energy, where kT_0 is the width of the trap distribution and is often called the Meyer-Neldel energy (E_{MN}) [8].

Fig. 5 shows that the width normalized parasitic resistance versus inverse of temperature was plotted based on the extracted R_p from $R_{on} \cdot W$ versus channel length plots measured at the temperature ranging from 293 to 323 K. The result indicates that R_p has thermally activated behavior, which means that R_p depends on the temperature as well as on gate-source voltage. Arrhenius plots indicate that the slope in Fig. 5(b) is steeper than that of Fig. 5(a) at the same gate-source voltage.

Fig. 6 shows that activation energy of OTFTs for S-80 and S-20 at each gate-source voltage was obtained from the slopes of the Arrhenius plots in Fig. 5. From least-square fitted lines in Fig. 5, the activation energy for S-80 is in the range from 42 to 48 meV, whereas S-20 has the range from 72 to 108 meV. The result indicates that the activation energy for R_p has the characteristics of grain size dependency. The grain size dependency on activation energy of R_p is also reported in the recent literature [20]. Even though different gate insulators are used for the reported OTFTs in the literature [20], the maximum pentacene grain sizes observed on SiO_2 and Al_2O_3 are approximately 10 and 40 μm , respectively. In the literature [20], the activation

energy for R_p was all within the range of 15–25 meV on Al_2O_3 , whereas the activation energy for SiO_2 were in the range from 20 to 40 meV. We notice that the activation energy for R_p in this study has the similar behavior of grain size dependency on R_p , compared with the result in the literature [20]. On the other hand, the activation energy in this study is largely higher than that in the literature [20]. The result is thought to be due to the fact that pentacene grain size in this study is much smaller than that in the literature [20].

In addition, the gate voltage dependency on activation energy for R_p can be explained by fact that the applied gate voltage in the TFTs moves the Fermi level through the trap distribution, closer to the band edge, which increases the effective mobility in pentacene. In polycrystalline pentacene, we consider the existence of trap states localized mainly at grain boundaries, which are distributed in higher energy levels than those in the grain. Such a model of trap distribution is also assumed in multiple trapping and thermal release, or variable-range hopping theory that explains carrier behavior in disordered organic transistors. The distributed trap states are occupied by gate-induced holes from a higher level with increasing carrier density, hence the determination by gate voltage of the state occupations. Therefore, increasing applied gate voltage lowers the activation energy, exciting holes at the lowest occupied state in deep traps to a conductive state. This model can easily explain the decreasing activation energy behavior of the polycrystalline devices as the gate bias was increased [22].

Since R_p is dominantly determined by sR_b and dR_b related with the bulk transport of pentacene, the gate voltage dependency on the effective mobility has naturally resulted in the characteristics of gate voltage dependency on R_p . In addition, the rate at which the activation energy (E_A) decreases with increasing gate voltage is an indicator of the density of trap states near the Fermi level [23]. As shown in Fig. 6, the rate for S-20 is higher than that of S-80. The result substantiates the fact that grain boundary trap density for S-20 is about two times larger than that of S-80. The different activation energy for S-80 and S-20 can be explained by the difference of N_t based on the above model. Therefore, R_p is critically dependent of grain size of pentacene, which determines the N_t related with pentacene bulk transport of pentacene.

Finally, another important consideration for the origins to determine R_p is the fact that band structure calculations for different polymorphs of pentacene have shown a significant dependence of the transport properties on even small changes in the pentacene crystal structure [12,13]. Therefore, the observed R_p difference between two samples could be at least partly related to slightly different film morphologies caused by different substrate temperature during pentacene deposition.

4. Conclusion

For top-contact OTFTs, contact resistance can be equivalently modeled as parasitic resistance (R_p) of a series of four resistive elements such as sR_i , sR_b , dR_b , and dR_e , which were originated from the charge injection/extraction process in the

S/D electrodes and the bulk transport in the pentacene. The pentacene grain size and its film morphology are critically correlated with the R_p because both sR_b and dR_b caused by bulk transport in pentacene contribute significantly to the value of R_p . The minimum effective contact resistance of $(R_p \cdot W)_0$, extracted from channel resistance method, has been tried to find the linkage of sR_i and dR_e originated from the injection/extraction at S/D electrodes because both sR_i and dR_e do not have the dependency on V_{GS} and are possibly affected by the effective channel width (W_{eff}) due to the surface morphology of pentacene. In addition, R_p is substantially influenced by grain boundary trap density (N_t), which are inversely proportional to the grain size for pentacene. The result is backed up by the fact that the activation energy for S-20 and S-80 confirms the relation of grain boundary trap density (N_t).

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