Depletion-Enhanced Body-Isolation (DEBI) Array on SOI for Highly Scalable and Reliable NAND Flash Memories

Il Han Park, Tae Hun Kim, Seongjae Cho, Jung Hoon Lee, Jong Duk Lee, *Member, IEEE*, and Byung-Gook Park, *Member, IEEE*

***Abstract*—A novel array architecture [depletion-enhanced body-isolation (DEBI)] has been proposed for NAND-type flash memories, and its memory characteristics are investigated in detail by device simulations. Having the shallow junctions on the thin active area, the proposed array architecture achieves high device performances with a fully depleted silicon-on-insulator (FDSOI) structure and enables stable erase operation without any problems based on an SOI structure. In particular, during the program operation, the DEBI architecture exhibited excellent self-boost efficiency originating from the isolated body. This can reduce the program disturbance effectively and can lower the V_{pass} voltages.**

***Index Terms*—Array, depletion-enhanced body-isolation (DEBI), disturbance, flash, NAND, self-boost, silicon-on-insulator (SOI).**

I. Introduction

RECENTLY, mobile applications are demanding high-density NAND flash memories, but issues of the equivalent oxide thickness (EOT) scaling down of flash cells due to the data retention make it difficult to reduce the short-channel effects in the deep submicrometer regime [1], [2]. To overcome this problem, several memory cells are developed with a fully depleted silicon-on-insulator (FDSOI) structure to reduce the short-channel effects [3], [4]. However, since it is hard to bias the floating body of memory cells, a reliable erase operation is not easy for an SOI-based NAND flash technology.

In this study, we report a depletion-enhanced body-isolation (DEBI) array architecture for a NAND-type flash memory based on an SOI technology. By biasing the bulk through the conducting path under the shallow junctions, the DEBI array (Fig. 1) enables block erase operation while maintaining the merits of the FDSOI structure. Moreover, the fully depleted body can increase the self-boost efficiency remarkably. After all, the DEBI architecture can be free from the program disturbance problem, which is one of the critical issues in a highly scaled NAND flash memory [5].

Manuscript received June 30, 2005; revised November 28, 2005. This work was supported by the Tera-bit Level Nano Device Project. The review of this paper was arranged by Guest Editor M. Tabe.

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Digital Object Identifier 10.1109/TNANO.2006.869951

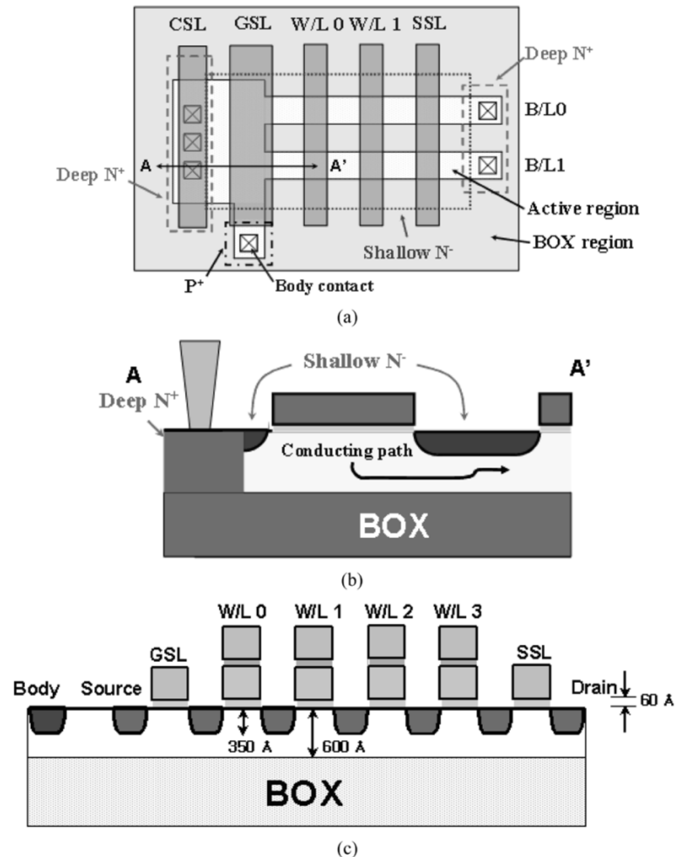

Fig. 1. Proposed DEBI structure. (a) Plan view. (b) Cross-sectional view of A-A'. (c) Simulated array structure. Body bias can pass through the conducting path under the shallow N$^-$ junction regions. $L_{\mathrm{gate}} = 60$ nm, $T_{\mathrm{TOX}} = 60$ Å, $X_J = 350$ Å, and $T_{\mathrm{Si}} = 600$ Å, respectively.

II. Array Architecture

Fig. 1 shows the proposed DEBI architecture. Basically, the DEBI array is fabricated on an SOI wafer. The active regions are defined by Si cutting, and bit lines (B/Ls) are isolated by the BOX regions. A thin active region is used for the fully depleted SOI structure. A p$^+$-doped active area is located at the side of the gate select line (GSL) [see Fig. 1(a)] to bias bulk potential. Also, to make a conducting path under the source/drain (S/D) extension regions, the shallow n$^-$ junctions are formed [see Fig. 1(b)]. Since only one body contact is needed for each sector, the density loss from the body contact is very small. Also, because the S/D extension regions of a NAND array are contactless,

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TABLE I
OPERATION SCHEME OF THE DEBI ARRAY. THE DEBI ARRAY CAN OPERATE WITH THE LOW V_{pass} VOLTAGE OF 4 V DURING THE PROGRAM OPERATION

	Erase	Program	Read
Sel. W/L	0	15	0
Pass W/L	0	4	4
SSL	F	V_{CC}	4
GSL	F	0	4
CSL	F	0	0
"0" B/L	F	0	1.2
"1" B/L	F	V_{CC}	<0.8
Bulk	15	0	0

the shallow junction formation can be possible. In particular, all of the processes are compatible with the conventional flash and SOI technology. That makes the proposed architecture easily realizable.

Two-dimensional and two-carrier simulation was performed by ATLAS. The simulated DEBI structure is shown Fig. 1(c). Four flash cells are connected in series with two select transistors. A T_{Si} of the array is 600 Å to make the body regions fully depleted during the read operation. The depth of the S/D extension regions is 350 Å to maintain a conducting path under the S/D regions and to improve the device performances by shallow junctions. The gate length is defined as 60 nm and the thickness of the tunnel oxide is 60 Å for reliable data retention characteristics, and the coupling ratio is fixed at 0.65. Simulated doping concentration of the shallow n$^-$ region is 5×10^{18}/cm^3 to prevent junction breakdown and that of the body region is at most 2×10^{18}/cm^3 with a Gaussian profile. The doping concentration of deep n$^+$ (for the common source line (CSL) and B/L contact) is 1×10^{20}/cm^3 and that of p$^+$ (for the body contact) is the same concentration. Also, the conventional NAND structure (replace BOX with Si) has been simulated for the comparison.

III. MEMORY OPERATIONS

The main operations of NAND flash memory are read, program, and erase. Table I indicates the operating bias scheme of the DEBI array. All of the bias is the same as that of the conventional NAND array except for the V_{pass} voltage during the program operation. In the DEBI architecture, the operation state determines the conductivity of the bulk bias to memory cells. During the read or program operation, the direct conducting path between the bulk bias and the memory cell is disconnected due to the fully depleted body region. The bulk bias has an influence on the channel potential of memory cells by the capacitance which is composed of a depletion region. However, this capacitance is much smaller than the gate capacitance, so the effect of bulk bias on the channel potential is very slight. That is, the body isolation of the memory cell is enhanced by the depletion region. However, during the erase operation, all of the channels are in accumulation mode, and the body bias can be connected to each cell directly through the conducting path under the shallow S/D extension regions. These effects are the key operation mechanisms of the DEBI architecture, and, due to these, a low V_{pass} voltage operation of the DEBI architecture is possible.

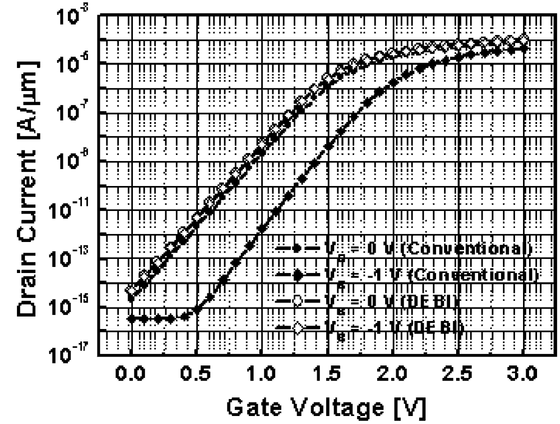

Fig. 2. I_D–V_G curves of the DEBI array cells and conventional bulk-type NAND array cells with 0 and -1 V of body bias. Cells in the DEBI array show no body effects.

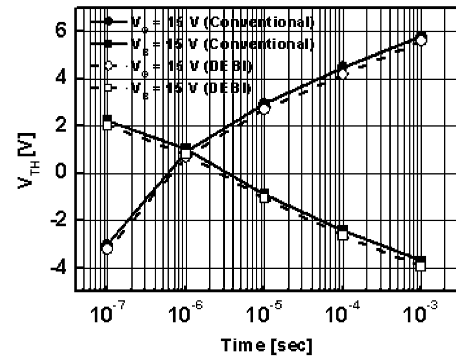

Fig. 3. Program and erase characteristics of cells in (a) the DEBI array and in (b) a conventional array. $V_B = 15$ V is used for the erase operation and $V_{\text{pgm}} = 15$ V for the program operation. A V_{pass} voltage is used at 4 and 9 V for the DEBI array and a conventional array, respectively.

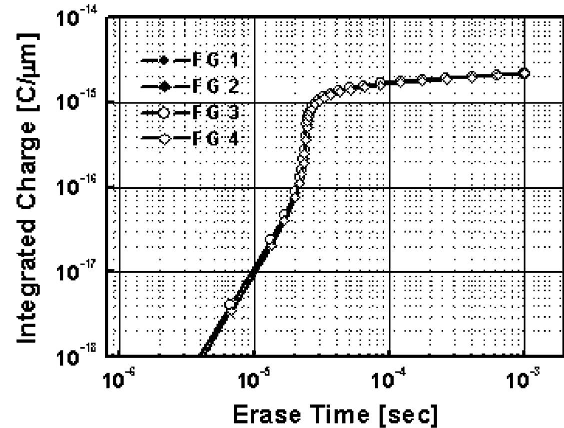

Fig. 4. Integrated charge of the DEBI cell's floating-gate curve during the erase operation. This result shows that the integrated charge of each floating gate has almost the same value during the erase operation.

Fig. 2 shows I_D–V_G characteristics of cells with different body voltages in the DEBI array and in the conventional NAND array. No body effect is shown in the DEBI array. In this way, the DEBI structure is operating virtually as an FDSOI structure during the read operation. An FDSOI structure and shallow junctions improve device performances and make the DEBI

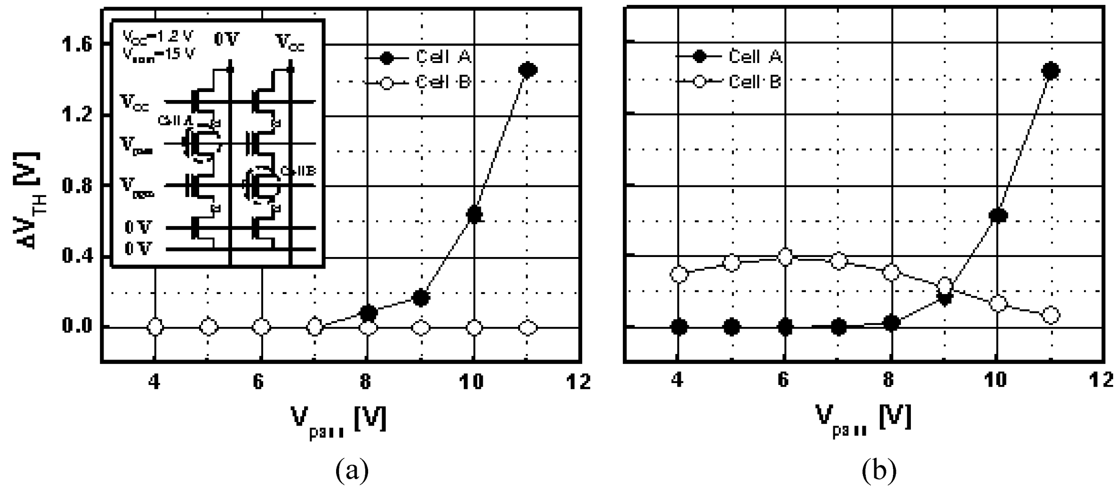

Fig. 5. Program disturbance of: (a) DEBI cell and (b) conventional array as a function of V_{pass}. $V_{\mathrm{CC}} = 1.2$ V and $V_{\mathrm{pgm}} = 15$ V is used for program operation.

array highly scalable. However, a more scaled DEBI array can have the low current issues from shallow and low-doped junction regions, but we can still solve that problem by using process techniques such as silicidation or a recessed channel structure.

The general nonvolatile-memory (NVM) base on an SOI structure does not have a body contact. Thus, the erase operation is commonly carried out by S/D-to-gate Fowler–Nordheim (FN) tunneling [1], [3], [4], but the contactless S/D extension regions render this method unsuitable for a NAND array. However, in the DEBI array, the body bias can be connected with each memory cells during the erase operation. This fact enables stable erase operation in the DEBI array. In Fig. 3, the DEBI array shows the same erase efficiency as the conventional one. Although in usage of narrow and shallow body conducting path, the body-to-gate current during the erase operation is very small ($<10^{-10}$ A/μm), and a potential drop problem can be negligible. Fig. 4 shows that the integrated charge of each floating gate has almost the same value during the erase operation.

In a NAND array, the self-boosting scheme [6] is used to prevent program disturbances. The program disturbance of V_{pgm} cell (the program inhibited cell shares the word line of the program cell) is determined by the boosted channel potential of the V_{pgm} cell. Fig. 5(a) and (b) shows the program disturbance of both a DEBI array cell and a conventional array cell, respectively, as a function of V_{pass} with a program voltage of 15 V. All of the cells, excluding the V_{pass} cell (cell A) and the V_{pgm} cell (cell B), in both arrays are erased cells. Because of the body isolation effect in the DEBI array, the channel potential of cell B in the DEBI array is self-boosted to 8.0 V when we bias only 4 V of small V_{pass} voltages, but the channel potential of cell B in a conventional scheme can be boosted to 7.4 V with 9 V of high V_{pass} voltages. Also, the V_{TH} shift of a V_{pgm} cell (cell B) in the DEBI array is 0.005 V despite a low V_{pass} voltage of 4 V (V_{pass} voltage of 4 V is the minimum voltage to turn off the programmed cell in order to transfer zero potential to the channel of the program cell.). Also, a low V_{pass} voltage reduces the V_{pass} disturbance of cell A. This program disturbance is the smallest compared to those of reported NAND structures [7], [8] with small program disturbance. This disturbance immunity can remove the number of program (NOP) problem completely. Also, the use of low V_{pass} voltage enables a simple operation circuit design.

IV. Conclusion

We have proposed a new DEBI array architecture for the NAND flash array. To enhance the body isolation by the depletion regions, the DEBI structure can improve the device performances and achieve a disturbance-free program scheme with a low V_{pass} voltage. With a simple array structure, high scalability, and high reliability, this architecture can be a promising candidate for next-generation NAND flash memories.

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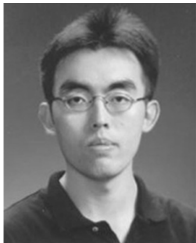

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