

Performance Improvement of Scaled-Down Top-Contact OTFTs by Two-Step-Deposition of Pentacene

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Abstract—When scaling down to the channel length (L_c) of 1.8 μm using a membrane shadow mask, top-contact pentacene thin-film transistors (TFTs) show that grain size dependency on the anomalous leakage current becomes conspicuous as L_c is comparable to the grain size. For scaled-down OTFTs with large and small grain, the obvious difference of off-current in the depletion regime can be attributed to various reasons such as pentacene conductivity, parasitic resistance, locally ill-defined source/drain edge, and Au interdiffusion. To improve mobility as well as $I_{\text{on}}/I_{\text{off}}$ ratio for scaled-down OTFTs, two-step-deposition (TSD) technique that enables us to control the channel conductivity in the depletion and accumulation regime as well as to improve the film continuity was proposed. To the best of our knowledge, the $I_{\text{on}}/I_{\text{off}}$ ratio of 10^7 and the mobility of $0.20 \text{ cm}^2/\text{V}\cdot\text{s}$ for OTFTs with L_c of 1.8 μm deposited by using the TSD technique was one of the best results in the literature.

Index Terms—Membrane shadow mask, top-contact pentacene thin-film transistors (TFTs), two-step deposition (TSD).

I. INTRODUCTION

RECENTLY, scaling-down approaches for organic thin-film transistors (OTFTs) have been highly demanded to obtain high current output capability and switching speed [1]–[4]. As the channel length decreases, electrical properties of contacts between the source/drain electrodes and the organic semiconductor become increasingly important to device performances [3], [4]. Therefore, it is meaningful to investigate how the device configuration (i.e., top- or bottom-contact) affects the performance of scaled-down OTFTs, because the contact properties can be critically determined by the configuration, which governs the film morphology of an organic semiconductor in the vicinity of the channel edge [5]. However, top-contact OTFTs are not favorably shrunk and frequently given to the chance to monitor the scaled-down effects due to the chemical fragility of most organic semiconductors, compared with bottom-contact OTFTs [6], [7].

In this letter, scaling down of top-contact pentacene TFTs was accomplished up to 1.8 μm by using a Si nitride membrane shadow mask [8]. Among various scaling-down phenomena, pentacene grain size effects on off-current were mainly studied

for the scaled-down top-contact pentacene TFTs. In addition, the two-step-deposition (TSD) technique, based on controlling pentacene growth parameters [9], [10] such as substrate temperature (T_s), deposition rate (DR), and pentacene film thickness (t_p), was proposed to improve the output current level as well as to maintain low off-current for the scaled-down OTFTs.

II. DEVICE FABRICATION

Top-contact OTFTs were fabricated on a p-type wafer with a resistivity of $15 \Omega\cdot\text{cm}$. After thermal oxidation, the oxide of 35 nm was patterned by photolithography and then etched by dilute HF solution for a contact of gate electrode. After surface modification by dilute PMMA solution [11], the as-received pentacene (Sigma Aldrich) with 97 % purity was thermally evaporated on the PMMA treated oxide under the vacuum level of 10^{-8} torr.

Split samples such as sample-20 (S-20), sample-80 (S-80), and sample-TSD (S-TSD) were fabricated by controlling pentacene growth parameters such as DR, T_s , and t_p . For two samples of S-20 ($T_s = 20^\circ\text{C}$) and S-80 ($T_s = 80^\circ\text{C}$), pentacene was deposited at the same conditions of DR = 0.3 $\text{\AA}/\text{s}$ and $t_p = 50 \text{ nm}$ except T_s . The TSD technique, modified from [12], was applied to the fabrication of S-TSD. The first layer of 10-nm-thick pentacene is deposited at $T_s = 80^\circ\text{C}$ and DR = 0.3 $\text{\AA}/\text{s}$ for the formation of large grain, and then the second layer of 40-nm-thick pentacene is deposited without vacuum break over the first layer at $T_s = 20^\circ\text{C}$ and DR > 5 $\text{\AA}/\text{s}$ to form intentionally the small grain layer [9], [10].

Finally, 50-nm-thick-gold was e-gun evaporated on the pentacene layer through a silicon nitride membrane shadow mask [8] to define source/drain (S/D) electrodes of OTFTs with the channel width (W_c) of 150 μm and the L_c ranging from 20 to 1.8 μm . Then, all electrical measurements for OTFTs without passivation were performed in air.

III. RESULTS AND DISCUSSION

For the S-80 and the S-20, the transfer characteristics in the saturation regime and the width-normalized device resistance as a function of channel length in the linear regime were shown in Fig. 1. Fig. 1(a) and (b) shows that the current level at $V_{\text{GS}} = V_{\text{DS}} = -20 \text{ V}$ in the saturation regime was significantly increased as L_c was reduced from 10 to 1.8 μm . For the OTFTs with L_c of 1.8 μm in Fig. 1(a) and (b), the effective mobility at $V_{\text{GS}} = -15 \text{ V}$ for S-80 and S-20 was 0.25 ± 0.05 and $0.08 \pm 0.02 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively. The result denotes that the

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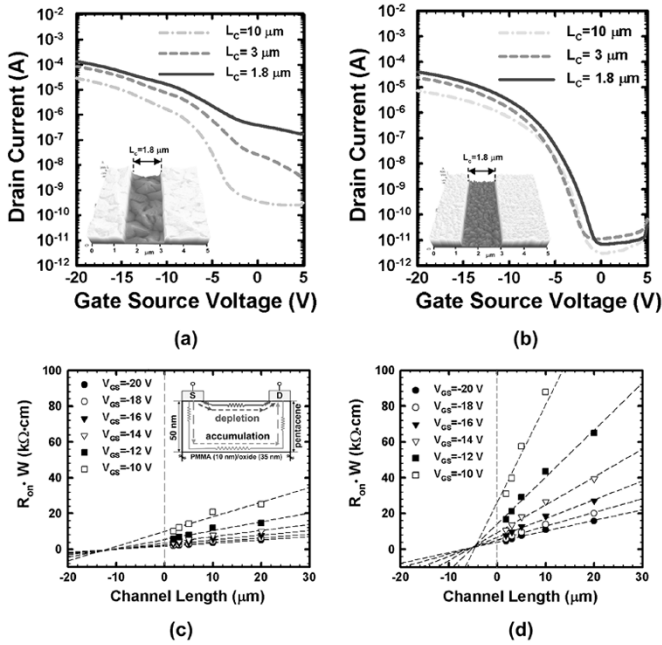


Fig. 1. Transfer characteristics for top-contact pentacene TFTs with deposition condition of (a) $T_s = 80^\circ\text{C}$ and (b) $T_s = 20^\circ\text{C}$ in the saturation regime ($W_c = 150\ \mu\text{m}$, $L_c = 10, 3$ and $1.8\ \mu\text{m}$, $V_{DS} = -20\ \text{V}$). The inset in Fig. 1(a) and in Fig. 2(b) shows that the AFM image of OTFTs with L_c of $1.8\ \mu\text{m}$ at $T_s = 80^\circ\text{C}$ and $T_s = 20^\circ\text{C}$, respectively. (c), (d) Width-normalized device resistance ($R_{on} \cdot W$) as a function of channel length (L_c) at $V_{DS} = -3\ \text{V}$ and gate voltage (V_{GS}) from -10 to $-20\ \text{V}$. $R_{on} \cdot W$ was extracted from top-contact OTFTs with channel lengths between 1.8 and $20\ \mu\text{m}$ and W_c of $150\ \mu\text{m}$. The y intercepts of the fitted dashed lines give the parasitic resistances at the various gate voltages. The inset in (c) illustrates the current path in the depletion regime as well as the accumulation regime.

mobility for S-80 is approximately three times larger than that of S-20, which is likely due to the grain size effects as shown in the insets of Fig. 1(a) and (b) [13].

As shown in Fig. 1(a), the increase of anomalous off-current in the depletion regime was reproducibly observed for the large-grain OTFTs as the channel length decreases to the size of pentacene grain, whereas a similar behavior of off-current was not observed for small-grain OTFTs, even with L_c of $1.8\ \mu\text{m}$. To investigate origins of anomalous off-current, the current path in the depletion regime as well as the accumulation regime was equivalently illustrated in the inset of Fig. 1(c). The inset indicates that holes injected from the source in the depletion regime prefer to pass through the top-path (depletion) rather than the bottom-path (accumulation) because of huge parasitic resistance at V_{GS} higher than $0\ \text{V}$.

The anomalous leakage current can be possibly determined by the various reasons such as pentacene conductivity, contact resistance, locally ill-defined S/D edge, and Au interdiffusion into pentacene. A study on the above-mentioned reasons may help elucidate the mechanism governing the off-current. Therefore, the conductivity for pentacene film was estimated using two probe measurements at $V_{GS} = 0\ \text{V}$ and $V_{DS} = -3\ \text{V}$, which produce fairly accurate results, as shown for OTFTs [14], [15]. The estimated conductivity of pentacene films for S-80 and S-20 were $(4.7 \pm 3.2) \times 10^{-6}\ \text{S/cm}$ and $(2.4 \pm 1.7) \times 10^{-8}\ \text{S/cm}$, respectively. The result indicates that the low conductivity for S-20 can be one of main reasons for low leakage current in the depletion regime, compared with that of S-80.

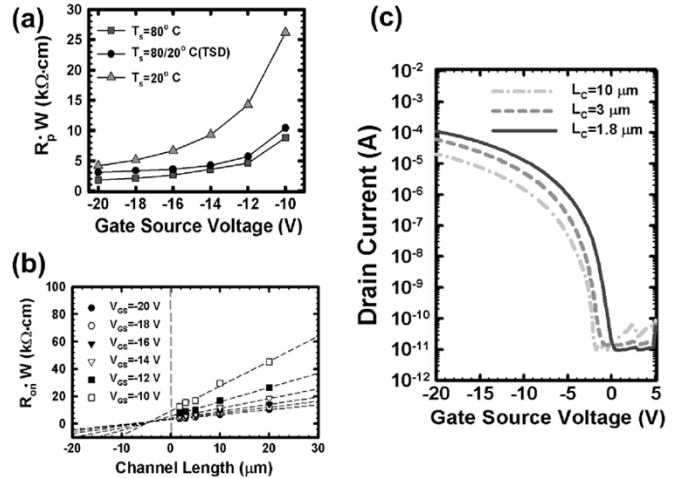


Fig. 2. (a) Width-normalized parasitic resistance ($R_p \cdot W$) as a function of gate voltage for OTFTs with pentacene deposited at $T_s = 80^\circ\text{C}$, $T_s = 20^\circ\text{C}$ and $T_s = 80/20^\circ\text{C}$ (TSD). (b) Width-normalized device resistance ($R_{on} \cdot W$) as a function of channel length (L_c) for OTFTs with pentacene deposited at $T_s = 80/20^\circ\text{C}$. (c) Transfer characteristics for pentacene TFTs with deposition condition of $T_s = 80/20^\circ\text{C}$.

The parasitic resistance (R_p) can be extracted by determining R_{on} from the linear regime of the transfer characteristics and plotting the width-normalized $R_{on} \cdot W$ as a function of L for different gate voltages [4]. From the $R_{on} \cdot W$ plot as shown in Fig. 1(c) and (d), the R_p , extracted at the y -axis intercept of the extrapolated linear fit of $R_{on} \cdot W$ versus L , was plotted in Fig. 2(a). Fig. 2(a) shows that the $R_p \cdot W$ for S-80 and S-20 at $V_{GS} = -16\ \text{V}$ is $2.6 \pm 0.3\ \text{k}\Omega\text{-cm}$ and $6.7 \pm 0.4\ \text{k}\Omega\text{-cm}$, respectively. As shown in Fig. 2(a), the R_p for S-80 in the accumulation regime is in the range of the value which is three times smaller than that of S-20. Considering the magnitude of R_p in the vertical direction, the conductivity/resistance in the horizontal direction between the source and drain is thought to be dominant in achieving the presented characteristics for the anomalous leakage current.

In addition, the interdiffusion of gold into pentacene film can influence the hole injection barrier height due to the interface dipole, which is substantially modified by the presence of organic adsorbates on Au electrodes [16]. Thus, the injection barrier height for contact of S-20 is thought to be higher than that of S-80 because the reaction area for S-20 is possibly larger than that of S-80. Besides, comparing with the rough surface of S-80, the smooth surface of S-20 may reduce the locally ill-defined S/D edge, which can be the source of the leakage path.

To reduce the anomalous off-current as well as obtain high mobility for scaled-down OTFTs, the TSD technique was proposed to obtain the high channel conductivity in the accumulation regime, the low lateral conductivity in the depletion regime, and the improved roughness of pentacene film. As shown in Fig. 3(d), the AFM image indicates that the high channel conductivity in the accumulation regime can be obtained due to the large grain size of 10-nm -thick pentacene deposited at $T_s = 80^\circ\text{C}$. On the other hand, AFM image in Fig. 3(c) shows that the small pentacene grain less than the size of $1\ \mu\text{m}$ by using the TSD technique can be intentionally topped over the large grain of pentacene in order to obtain the improved film continuity and the low conductivity of pentacene in the depletion regime.

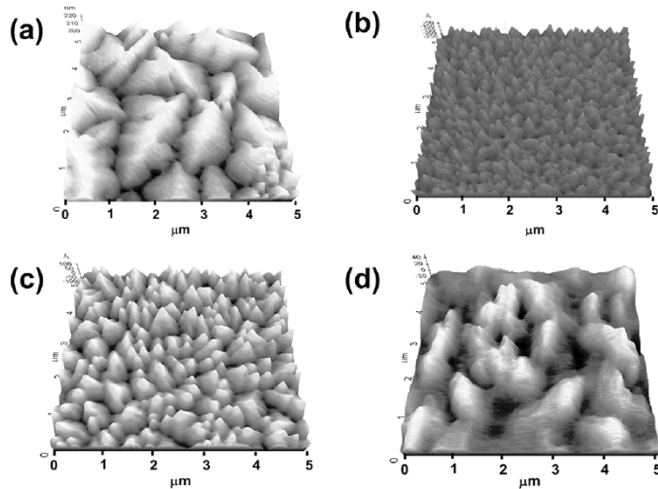


Fig. 3. AFM images of pentacene layer for samples such as (a) S-80, (b) S-20, and (c) S-TSD. For each sample except sample (d), pentacene has the thickness of 50 nm. (d) AFM image for 10-nm-thick pentacene film deposited at a rate of 0.3 Å/s on the condition of $T_s = 80^\circ\text{C}$, indicating that large-grain pentacene of a few micrometers in size was formed at the insulator/pentacene interface.

Transfer characteristics of devices for S-TSD were shown in Fig. 2(c). The obvious difference is that the anomalously high off-current was not observed for scaled-down OTFTs even with an L_c of 1.8 μm . Compared with the electrical performance of the S-80 device with L_c of 1.8 μm , the $I_{\text{on}}/I_{\text{off}}$ ratio and sub-threshold slope (SS) were conspicuously improved from 10^3 to 10^7 and from 5.3 ± 0.5 V/dec to 2.0 ± 0.3 V/dec, respectively. However, the field-effect mobility (μ_{eff}) and the threshold voltage (V_{th}) were slightly changed from 0.25 ± 0.05 $\text{cm}^2/\text{V}\cdot\text{s}$ to 0.20 ± 0.02 $\text{cm}^2/\text{V}\cdot\text{s}$ and from -3.0 ± 0.2 V to -3.5 ± 0.3 V.

From the $R_{\text{on}} \cdot W$ plots for S-TSD as shown in Fig. 2(b), $R_p \cdot W$ in the accumulation regime was obtained in Fig. 2(a). Fig. 2(a) shows that the reduced mobility for S-TSD is attributed to the slightly increased parasitic resistance from 2.6 ± 0.3 to 3.6 ± 0.2 $\text{k}\cdot\Omega\cdot\text{cm}$ at $V_{\text{GS}} = -16$ V. By using the two probe measurements as mentioned before, the conductivity for S-TSD was obtained as $(3.2 \pm 2.1) \times 10^{-8}$ S/cm, which is similar to the conductivity for S-20. Fig. 3(c) shows that the improved surface roughness by TSD is closely related to the noticeable reduction of leakage current caused by the ill-defined S/D edge. Moreover, the hole injection barrier height in the depletion regime for S-TSD is thought to be increased to the similar value of S-20 due to the increase of reaction area, compared with S-80.

IV. CONCLUSION

As L_c scales down to a length comparable to the grain size of pentacene, the anomalous leakage current for scaled-down OTFTs was reproducibly observed in the depletion regime and has a dependency on pentacene grain size. Among various factors, the leakage current in the depletion regime can be mainly determined by the channel conductivity in the depletion regime,

the locally ill-defined S/D edge, and injection barrier height by gold diffusion into pentacene. The TSD technique can be one of several possible ways to obtain good mobility and high $I_{\text{on}}/I_{\text{off}}$ ratio for scaled-down OTFTs.

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